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AUTHOR – AUTEUR

Full Name of Author – Nom complet de l'auteur

ARUNA BOPAIAH AJJIKUTTIRA

Date of Birth – Date de naissance
1958 07 11

Canadian Citizen – Citoyen canadien
☐ Yes / Oui ☑ No / Non

Country of Birth – Lieu de naissance
REPUBLIC OF INDIA

Permanent Address – Résidence fixe
#5 REAR OUT HOUSE
SESHAMAHAL, V. V. PURAM
BANGALORE - 560 004, INDIA

THESIS – THÈSE

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University – Université
UNIVERSITY OF ALBERTA

Name of Supervisor – Nom du directeur de thèse
Dr. KEITH A. STROMSMOE

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by

ARUNA B. AJJIKUTTIRA

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled CMOS OPERATIONAL AMPLIFIERS submitted by ARUNA B. AJJIKUTTIRA in partial fulfilment of the requirements for the degree of MASTER OF SCIENCE.

Keith A. Stromsmoe

Supervisor

I. D. Calvert

Supervisor

John Salmon

W. Eisenmenger

Date 1985 04 11

Dedicated

To the loving memory of my mother

ABSTRACT

Many analog circuits such as switched-capacitor filters use a number of operational amplifiers as a part of the circuit. Such amplifiers are sometimes called internal operational amplifiers. In this thesis the design, simulation and performance of three CMOS internal operational amplifiers are discussed. SPICE simulation is used to study the circuit behaviour and select appropriate device sizes. The operational amplifiers were fabricated using the Northern Telecom CMOS-1B process. Results of the tests conducted on the fabricated chips are given, and they agree closely with the simulation results. Also a modification to the operational amplifier to make it sensitive to magnetic fields is described.

The first two chapters include the introduction and a discussion of the basic building blocks used in operational amplifiers. The next two chapters discuss the three operational amplifiers that were designed and the magnetic field sensor in detail. Chapter five addresses operational amplifier parameters and circuit techniques for their measurement. The last chapter discusses the results obtained and draws some conclusions.

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1. INTRODUCTION AND MOTIVATION

1.1 Brief Introduction to Operational Amplifiers

A feedback stabilized D.C. amplifier which has high input impedance, high gain, and low output impedance can be useful in many ways. By using different passive elements externally it can, for example, serve as an integrator, differentiator, adder or subtractor. Since such an amplifier can perform the mathematical operations of arithmetic and calculus on the voltages applied to its input, it is called as an 'Operational Amplifier' [1,2] (Op-amp for short).

The operational amplifier is one of the most useful analog circuit building blocks. In the simplest case it can be used as an amplifier for signals ranging from dc to a few MHz, where the net gain can be controlled by varying the feedback resistor. It can also be used to amplify differential signals. It can be used to form active filters, precision rectifiers, clippers, and waveform generators. Combining it with other active and passive elements we can obtain a number of other useful circuits.

Op-amps were originally realized using vacuum tubes. Next they were built using discrete components such as transistors, diodes, resistors and capacitors. Around 1963 the first monolithic Op-amps were built. In the following years, because of improved technology, Op-amps became more reliable and less costly. Presently we have a vast array of Op-amps specifically designed to suit a particular need.

1.2 Classification

Depending on the technology used, Op-amps can be classified into two broad categories : Bipolar Op-amps and MOS Op-amps. Bipolar Op-amps were the first to be developed and much work has been done in that field [3]. Most of the ideas in MOS Op-amps are borrowed from their bipolar counterparts. Generally bipolar Op-amps are superior when compared to MOS Op-amps, in particular with respect to gain. The transconductance g_m of a bipolar transistor is completely defined once the collector current is given - because of the exponential Current - Voltage characteristics of the p-n junction. Transconductance of a MOS transistor is given by

$$g_m = 2\sqrt{k'(W/L)ID} \quad \text{.....(1.1)}$$

where

$k' = (1/2)\mu C_{ox}$

μ = electron (hole) mobility

C_{ox} = gate oxide capacitance

W = width of the transistor

L = Length of the transistor

ID = Drain current

Figure 1.1 gives a plot of transconductance versus quiescent current for both bipolar and MOS transistors (with different W/L ratios). As can be seen bipolar transistors are superior to MOS transistors as far as transconductance is concerned.

Another way of classification of Op-amps is based on their application. There are two broad divisions in this

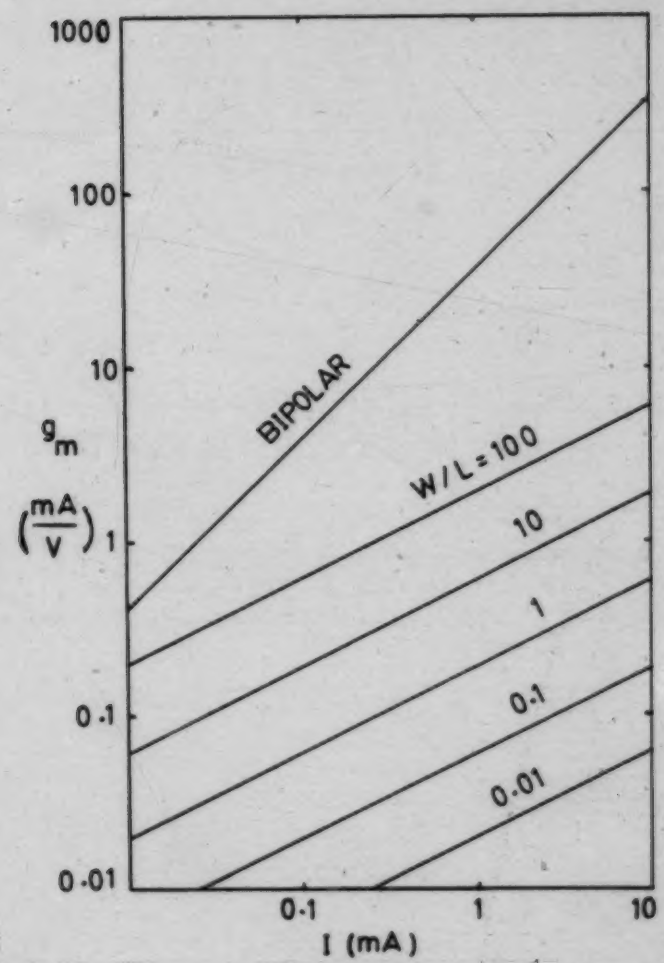


Figure 1.1 Transconductance as a function of quiescent current for MOS transistors of various values of W/L and for bipolar transistor [4]. MOS transistors in saturation, $k' = 10\ \mu A/V^2$

category - 'Stand-alone' Op-amps, and 'Internal' Op-amps. In the case of Stand-alone Op-amps, the whole chip area is used solely for the Op-amp circuit. Some characteristics of Stand-alone Op-amps are listed below :

* Generally of bipolar plus FET type
* Can deliver a good amount of power to the load
* Very high imput impedance
* Low output impedance
* Usually incorporate some protection circuit
* Dissipate considerable amount of power

These Stand-alone Op-amps can be further classified as General Purpose, and Special Purpose Op-amps. A classic example of the General Purpose Op-amp is the μA 741. Special Purpose Op-amps include the following types :

* High gain
* Gain control
* High Slew-rate
* Wideband
* Low noise
* Low drift
* Low offset

In the case of Internal Op-amps, the chip area is shared by different circuits. A good example would be switched-capacitor filters[5], where the complete circuit consists of a few Op-amps, and a number of capacitors. Here the Op-amps are part of the circuit - they need not have to deliver power to an external load. The load is known

beforehand and the output current requirements are usually low. This simplifies the design of internal Op-amps. For reasons to be discussed later in this chapter, Internal Op-amps are usually of MOS type.

1.3 Need for CMOS Op-amps

In recent years the digital field has grown by leaps and bounds. As a result of the tremendous growth in microprocessor and memory technology, a lot of processing power is at the disposal of designers. It is expected that the trend in the future is to integrate whole systems on a chip. The major role of analog circuits in the future is expected to be in the area of interface circuits. These circuits connect the 'Real World' of analog signals with the digital world of discrete and digitally encoded signals.

MOS technology has an important role to play in this trend toward system integration. The high density of circuit elements obtainable in MOS technology makes it possible to implement complex systems in modest chip areas. Of the two popular MOS technologies - NMOS and CMOS - the latter is better suited for VLSI systems in view of its high circuit density, better noise margin, low power consumption, and the availability of complementary devices[6]. Thus there is a need for the realization of analog circuitry using the traditionally digital technology of CMOS.

Keeping this in mind, a good topic for research in CMOS analog circuitry is CMOS operational amplifiers. As

mentioned earlier, Op-amps are by far the most frequently used subsystems in any analog system. Since complementary devices are available in CMOS technology, the results of the research in bipolar Op-amps can be used with advantage for CMOS Op-amp design.

Recently Northern Telecom Limited of Ottawa has offered to provide its CMOS fabrication facilities to Canadian Universities on a multi-project chip basis. With this facility there is new meaning to research in CMOS integrated circuits. Now it is possible to design *and test* one's circuit - the much needed 'hands-on' experience is available.

1.4 Thesis objectives

In view of the points mentioned above, it was decided to set the the following objectives for this thesis:

1. To design, simulate, and fabricate (using Northern Telecom process) some internal operational amplifier circuits.
2. Test the fabricated chips and compare the results with those obtained from simulation.
3. To try frequency compensation using MOS transistors instead of a resistor.
4. Explore the possibility of modifying Op-amps to function as magnetic field sensors

In the second objective we decided to test the following parameters of an Op-amp: input offset voltage, DC

open-loop gain, unity-gain frequency, output resistance, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), slew rate, and the power dissipation.

2. BASICS OF MOS OP-AMP DESIGN

In this chapter the basic building blocks required for MOS Op-amp design are discussed. Since this subject is very vast, only the important parts are chosen and discussed briefly.

2.1 MOS Inverting Amplifier

The starting point for MOS analog circuits is the basic MOS transistor amplifier. Figure 2.1 shows a simple MOS gain stage using n-channel enhancement mode MOSFET with a resistive load. Figure 2.2 shows the voltage-current characteristics of an n-channel MOSFET. The transistor has two distinct regions of operation :

(a) The ohmic or triode region where the tranisitor is operated with a low drain-to-source voltage VDS, such that VDS<(VGS-VTH). Here VGS is the gate-to-source voltage and VTH is the threshold voltage. In this region the device behaves in a manner similar to a voltage-controlled resistor.

(b) Saturation or pinch-off region, where the device is operated with sufficient drain-to-source voltage such that VDS>(VGS-VTH). In this region the MOSFET behaves as a voltage-controlled current source. This region is also known as the 'saturation region' since the drain current is saturated and is relatively insensitive to drain-to-source voltage VDS.

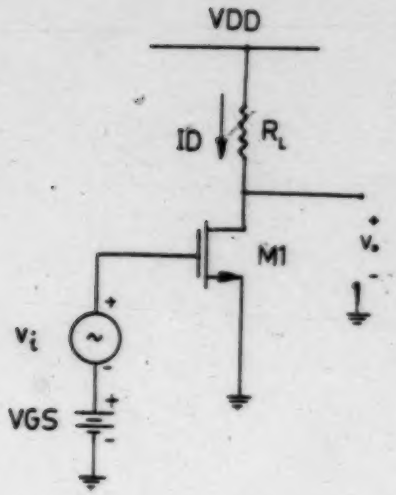


Figure 2.1 NMOS gain stage with resistive load

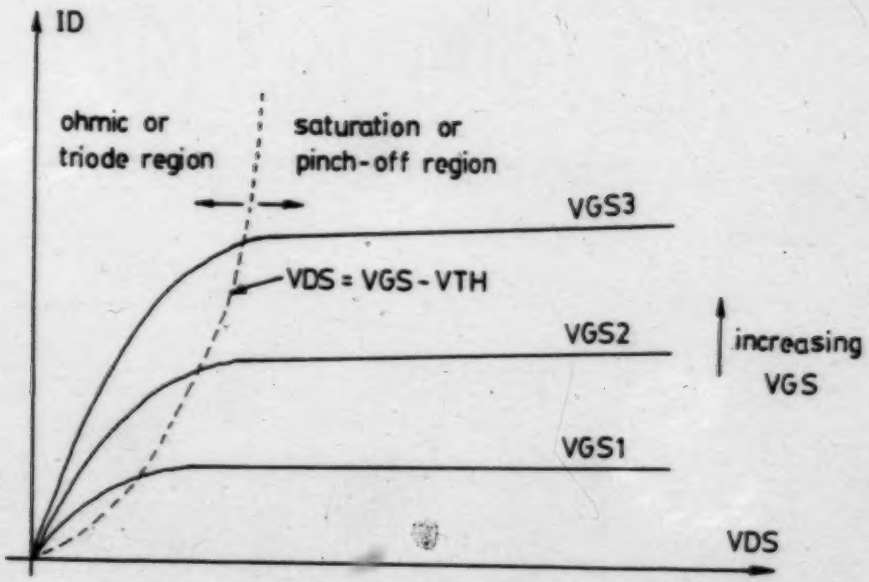


Figure 2.2 Voltage-Current characteristics of n-channel MOSFET

Assuming that the MOSFET is biased to operate in its pinch-off region, its drain current ID can be expressed by the equation

$$ID = (\mu C_{ox}/2)(W/L)(VGS-VTH)^2 \quad \text{.....(2.1)}$$

From this the transconductance g_m in the pinch-off region can be calculated as

$$g_m = \partial ID/\partial VGS = \mu C_{ox} (W/L)(VGS-VTH) \quad \text{.....(2.2)}$$

which can also be written as

$$g_m = \sqrt{2\mu C_{ox} (W/L) ID} \quad \text{.....(2.3)}$$

or

$$g_m = (2 ID)/(VGS-VTH) \quad \text{.....(2.4)}$$

From equation (2.3) we can see that the transconductance is proportional to the root of the aspect ratio (W/L), once the drain current is fixed. Thus the transconductance can be varied by varying the device geometry.

The μC_{ox} product is a process parameter which is fixed for a given MOS fabrication process. For the Northern Telecom Electronics (NT) CMOS-1B process [7],

$$\mu_n = 750 \text{ cm}^2/\text{V-sec}$$

$$\mu_p = 250 \text{ cm}^2/\text{V-sec}$$

$$C_{ox} = (4.06 \pm 0.24) \times 10^{-8} \text{ F/cm}^2$$

which gives

$$(\mu_p C_{ox} \cong 10 \ \mu\text{A/V}^2)$$

for p-channel devices, and

$$(\mu_n C_{ox} \cong 30 \ \mu\text{A/V}^2)$$

for n-channel devices.

We can compare the transconductance of a MOS transistor with that of a bipolar transistor. The collector current IC of a bipolar transistor can be expressed as

$$IC = I_o[\exp(qVbe/kT) - 1] \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.5)$$

where

I_o = reverse saturation current,

q = electron charge,

k = Boltzman's constant,

T = absolute temperature, and

Vbe = base-to-emitter voltage.

Assuming $[\exp(qVbe/kT)] >> 1$,

$$g_m = \partial IC/\partial Vbe = IC/V_T \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.6)$$

where $V_T = kT/q$.

From equations (2.2), (2.3), (2.4), and (2.6) we can see that

(a) The transconductance of a bipolar transistor is completely defined once its collector current is given. It does not depend on the device geometry.

(b) The transconductance of MOS device depends on (i) the aspect ratio (W/L), and (ii) gate-to-source voltage VGS or the drain current ID.

Figure 1.1 shows a plot of the transconductance of bipolar and MOS device as a function of the operating current. This gives a clue as to why bipolar Op-amps perform better than MOS Op-amps.

The voltage gain of the gain stage shown in Figure 2.1 can be shown to be

$$A_v = v_o/v_i = -g_m (R_L || r_o) \quad \text{.....(2.7)}$$

where r_o is the output resistance of the transistor M1.

2.2 Simple MOS Current Source

Current sources play an important role in analog integrated circuits as biasing elements. They are preferred over resistors since they perform better and occupy less chip-area.

Figure 2.3 shows a simple MOS current source, and figure 2.4 shows its voltage-current characteristics. The gate and drain of transistor M1 are shorted. Because of this, as soon as the gate-to-source voltage VGS exceeds the threshold voltage VTH for transistor M1, it enters the saturation region. The same VGS is applied to transistor M2. So if the transistors M1 and M2 are identical in every aspect, the drain current I_o of transistor M2 will be the same as the reference current, Iref. This is illustrated in figure 2.4. It can be seen that the current remains almost constant for different voltages of V_o, V_o>(VGS-VTH). This current I_o can be used to bias other circuit elements.

Using equation (2.1), we can obtain the design equation for simple current source as

$$I_o = [(W/L)_2/(W/L)_1].Iref \quad \text{..... (2.8)}$$

This circuit is sometimes called as 'Current Mirror' because if $(W/L)_2 = (W/L)_1$ in (2.8), I_o = Iref.

A single diode connected transistor, such as M1 of figure 2.3, can be used to establish different currents in

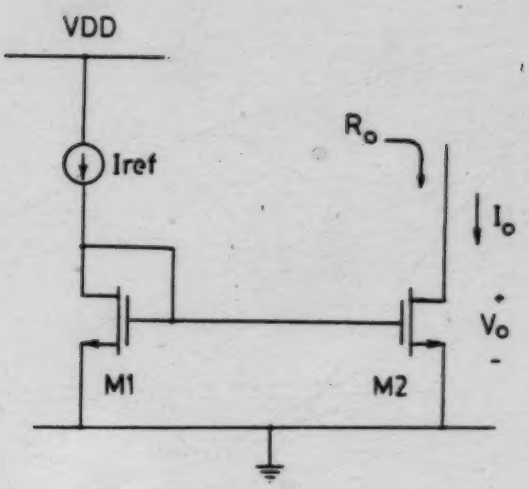


Figure 2.3 Simple MOS current source

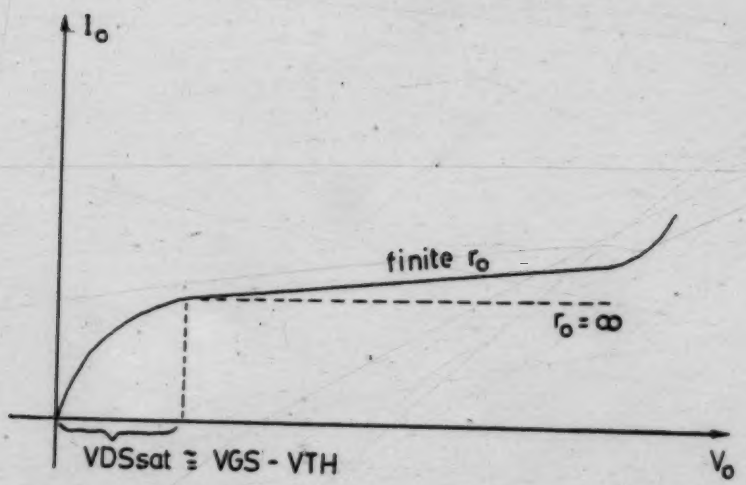


Figure 2.4 Voltage - Current characteristics of simple MOS current source

many branches. Since MOS transistors do not draw any gate current, this does not affect the performance of the current source. This may be compared with the bipolar current source where the finite base current limits the number of branches that can be added on.

One of the figure of merit of a current source is the output resistance R_o, as illustrated in figure 2.3. For a simple MOS current source,

$$R_o = r_{o2} = VA/I_o = 1/(\lambda I_o) \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.9)$$

where

r_{o2} is the output resistance of transistor M2,

VA (= $1/\lambda$) is the Early voltage of transistor M2, and

λ is the channel length modulation factor.

The channel length modulation factor, λ, depends on the length of the transistor, the substrate concentration, and the substrate bias.

2.3 Improved Current Sources

By adding extra transistors to the simple current source, its performance can be improved. Although many circuits exist, two important circuits are briefly discussed here.

2.3.1 Cascode Current Source

A cascode current source is obtained by stacking two or more simple current sources, one on top of the other, as

shown in figure 2.5. This provides higher output resistance and better current stability. The voltage - current characteristics for this circuit is shown in figure 2.6. The output resistance is given by

$$R_o = r_{o4}[(1 + (g_{m4} + g_{mb4})r_{o2}] + r_{o2} \quad \ldots\ldots\ldots (2.10)$$

where g_{mb4} is the transconductance due to the effect of source-to-substrate voltage on the drain current.

As indicated by equation (2.10) the output impedance increases considerably, compared to a simple current source. But this is not without a drawback. Because of stacking, the range of voltage swing at the output for which both transistors are in saturation is (VTH + 2VDSsat), which is a significant increase from VDSsat for simple current source. This limitation in output voltage swing puts an upper limit on the number of cascoding stages.

2.3.2 Wilson Current Source

This is another popular high-impedance current source. Figure 2.7 shows the schematic of the Wilson current source. Transistor M1 provides negative feedback which helps to increase the output resistance by approximately the same amount as the cascode current source.

An important aspect of Wilson current source is that for large values of threshold voltage the drain voltage of transistor M1 is higher than that of M2 by a volt or more, leading to large drain current mismatch due to the finite output resistance of the devices. To overcome this drawback

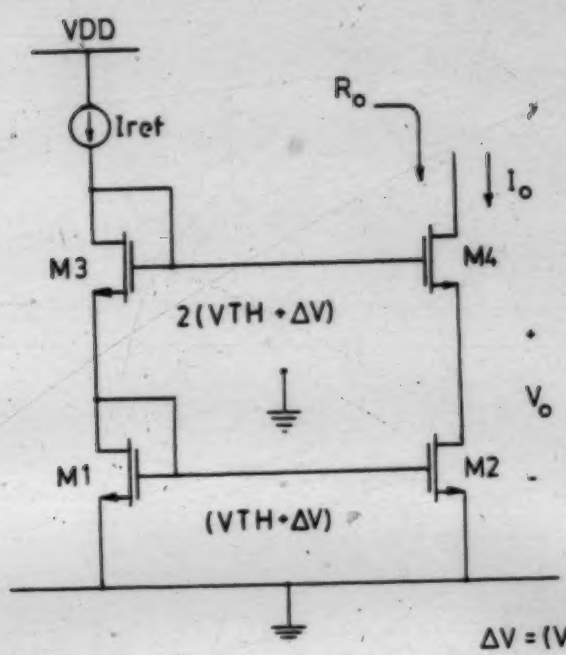


Figure 2.5 Cascode current source

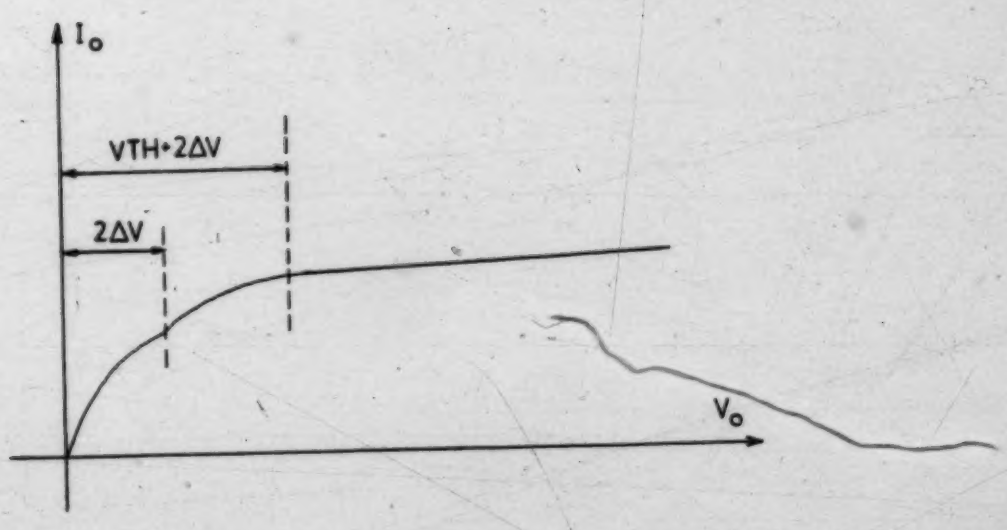


Figure 2.6 Voltage - Current characteristics of cascode current source

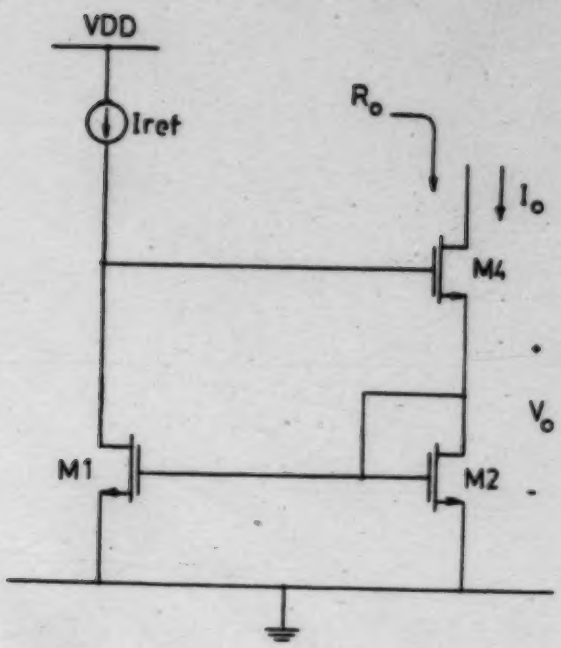


Figure 2.7 Wilson current source

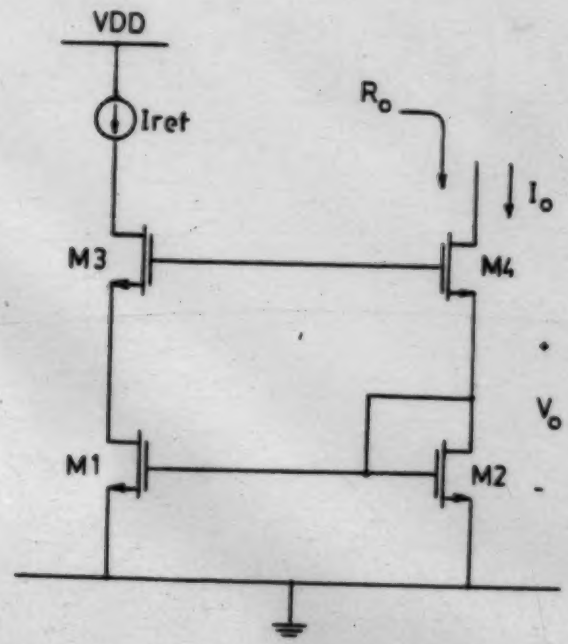


Figure 2.8 Improved Wilson current source with additional device to equalize the drain voltages of M1 and M2

an additional transistor M3 is usually included as shown in figure 2.8 to equalize the drain voltages.

The output resistance is approximately given by the equation

$$R_o \cong r_{o4} \cdot g_{m1} \cdot r_{o1} \quad \text{.....(2.11)}$$

2.4 The Body Effect

Consider the circuit of figure 2.9(a) and its implementation using Northern Telecom's p-well process CMOS-1B. The p-type transistors are made on the n-substrate of the wafer, and the n-type transistors are made in the p-well which is formed on the n-type wafer. Normally the source is connected to the substrate. But in the case of transistors M1 and M2, this is not possible. Assume that a typical drain-to-source drop of 3 volts exists on transistors M3, M4 and M5. Then the terminal voltages of transistors M1 and M2 are as shown in figure 2.9(b). Here the substrate is more positive with respect to the source. Thus we have a wider depletion region than normal, containing more fixed charges. This implies that for the same amount of surface charge in the channel, a higher electric field must exist in the oxide layer between the channel and the gate electrode. This in turn means we need more negative voltage on the gate to achieve the same number of charge carriers in the channel. The net result of this is an increase of the threshold voltage VTH as the reverse bias between the substrate and source is increased. This effect

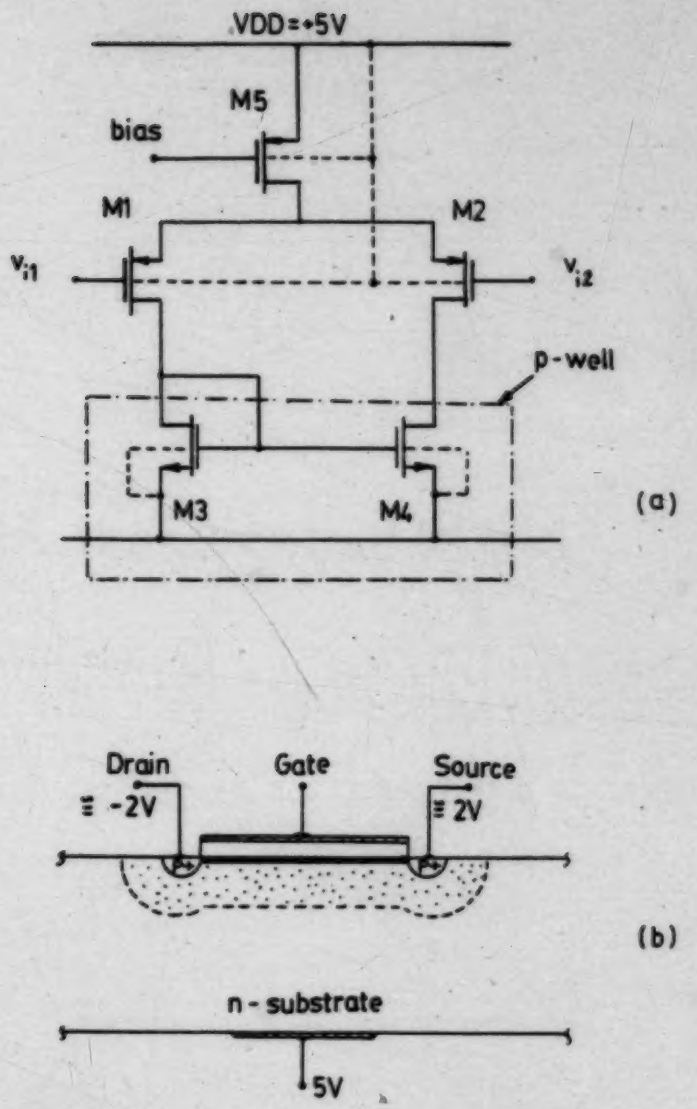


Figure 2.9 (a) Circuit to illustrate the body effect (b) Schematic of transistor M1

is called as the 'Body Effect'.

Figure 2.10 shows the variation of threshold voltage with substrate bias for the Northern Telecom CMOS-1B process, for a 50/25 microns transistor [7].

The dependence of threshold voltage on the source-body bias VBS gives rise to a body-effect transconductance g_{mb}. This is related to the actual transconductance g_m (due to the gate-voltage) as [4]

$$\lambda = g_{mb} / g_m \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.12)$$

where

$$\lambda = [2C_{ox}]^{-1} \cdot \sqrt{[(2q\epsilon_s NA) / (2\Phi_f + VSB)]} \quad \ldots\ldots\ldots (2.13)$$

Here Φ_f is the potential difference between the Fermi level and the intrinsic level in the substrate, ϵ_s is the dielectric constant of silicon, NA is the substrate impurity concentration. Note that the primary factors in determining λ are the substrate doping NA and the source-body bias VSB.

2.5 MOS Differential Pair

In this section the differential pair, which forms the heart of any Op-amp, is discussed briefly.

2.5.1 DC Transfer Characteristics

Figure 2.11(a) shows a simple MOS differential pair biased by a constant current source ISS. Assuming M1 and M2 to be matched devices, with equal W/L, the drain currents ID1 and ID2 can be written as

$$ID1 = k'(W/L)(VGS-VTH)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.14)$$

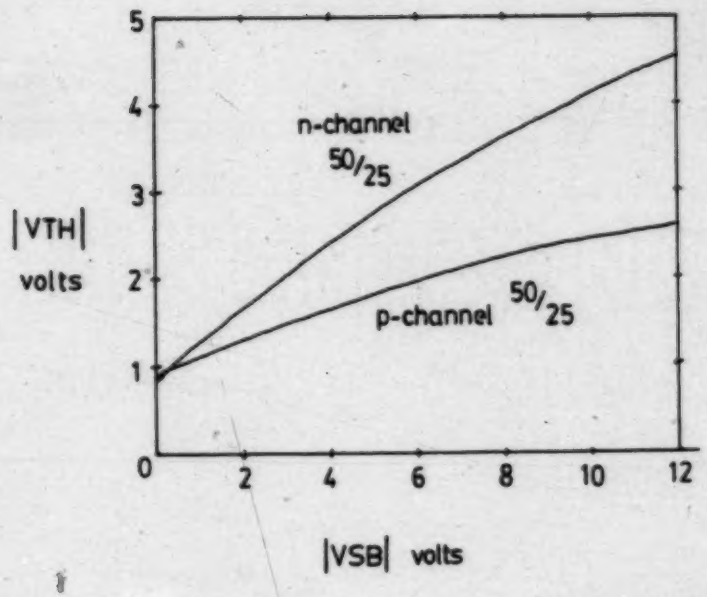
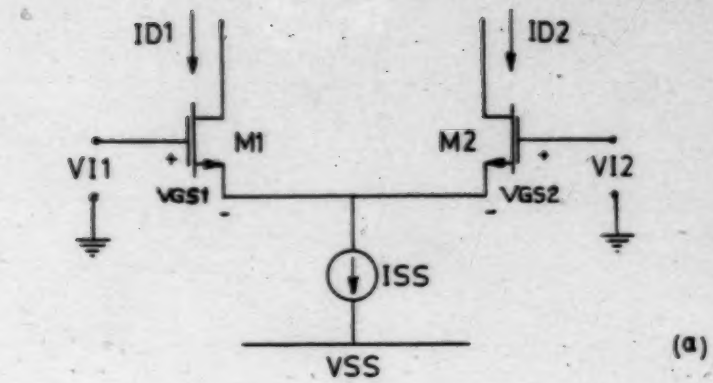


Figure 2.10 Threshold voltage versus substrate bias



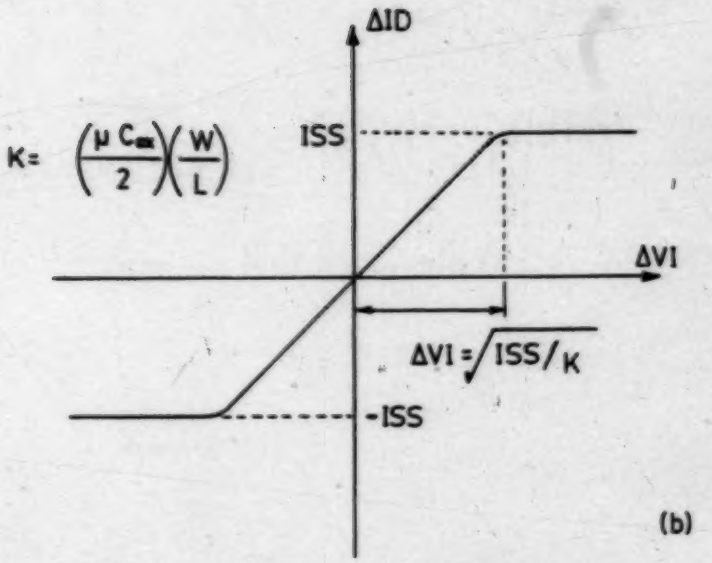


Figure 2.11 (a) Schematic of a MOS differential pair (b) Its DC transfer characteristics

$$ID2 = k'(W/L)(VGS-VTH)^2 \quad \text{.....(2.15)}$$

where $k' = (\mu C_{ox}/2)$.

The differential input voltage

$$\Delta VI = VI1 - VI2 = VGS1 - VGS2 \quad \text{.....(2.16)}$$

would appear as a net voltage difference between VGS1 and VGS2, and results in a differential current

$$\Delta ID = ID1 - ID2 \quad \text{.....(2.17)}$$

From equations (2.14) through (2.17) ΔID can be calculated, neglecting the body effect, as

$$\Delta ID \cong K\Delta VI \sqrt{(2.ISS/K) - (\Delta VI)^2} \quad \text{.....(2.18)}$$

where

$$K = (\mu C_{ox}/2)(W/L) = k'(W/L) \quad \text{.....(2.19)}$$

Equation (2.18) is valid as long as

$$|\Delta VI| \leq \sqrt{ISS/K} \quad \text{.....(2.20)}$$

This results in a dc transfer characteristics as shown in figure 2.11(b). When $|\Delta VI| > \sqrt{ISS/K}$, either M1 or M2 is off, and $\Delta ID = ISS$.

Note that increasing ISS causes the linear region of the transfer characteristics to increase, whereas increasing the (W/L) ratio decreases the linear region.

The transconductance G_m of the differential pair can be found by differentiating equation (2.18), as

$$G_m = \partial(\Delta ID)/\partial(\Delta VI)$$

$$= ISS(\mu C_{ox})(W/L) \quad \text{.....(2.21)}$$

or $$G_m = g_{m1} = g_{m2} \quad \text{.....(2.22)}$$

2.5.2 Small Signal Analysis

Figure 2.12(a) shows a CMOS differential stage with an active load. The small signal performance of this circuit may be studied by considering two signals v1 and v2 at the two input terminals, and treating them mathematically as v1 = (vic + vid/2) and v2 = (vic - vid/2). Here vic is the common input voltage [vic=(v1+v2)/2], and vid is the differential input voltage [vid=(v1-v2)]. Figure 2.12(b) shows the simplified equivalent circuit for this differential stage. The body effect has been neglected, and it is assumed that the drain-to-source resistance of transistors M1 and M2 is very large. Under these assumptions the output voltage may be expressed in terms of vic, vid, and other circuit parameters. This output voltage may then be seen as the sum of two gains - common mode gain (Acm) because of vic, and differential mode gain (Adm) because of vid.

For this circuit, using the equivalent circuit shown, it can be shown that

$$Acm = -\{[g_{m2}-(g_{m1}.g_{m4})/g_{m3}].r_{ds}\}/[1+(g_{m1}+g_{m2})r_{ds}] \quad ...(2.23)$$

The expression for Adm is quite involved, and if we further assume that transistors M1 and M2 are identical, and, M3 and M4 are identical then

$$Adm = g_{m2}.r_{ds} \quad ...(2.24)$$

From these two equations, another useful parameter called common mode rejection ratio, CMRR, is defined as

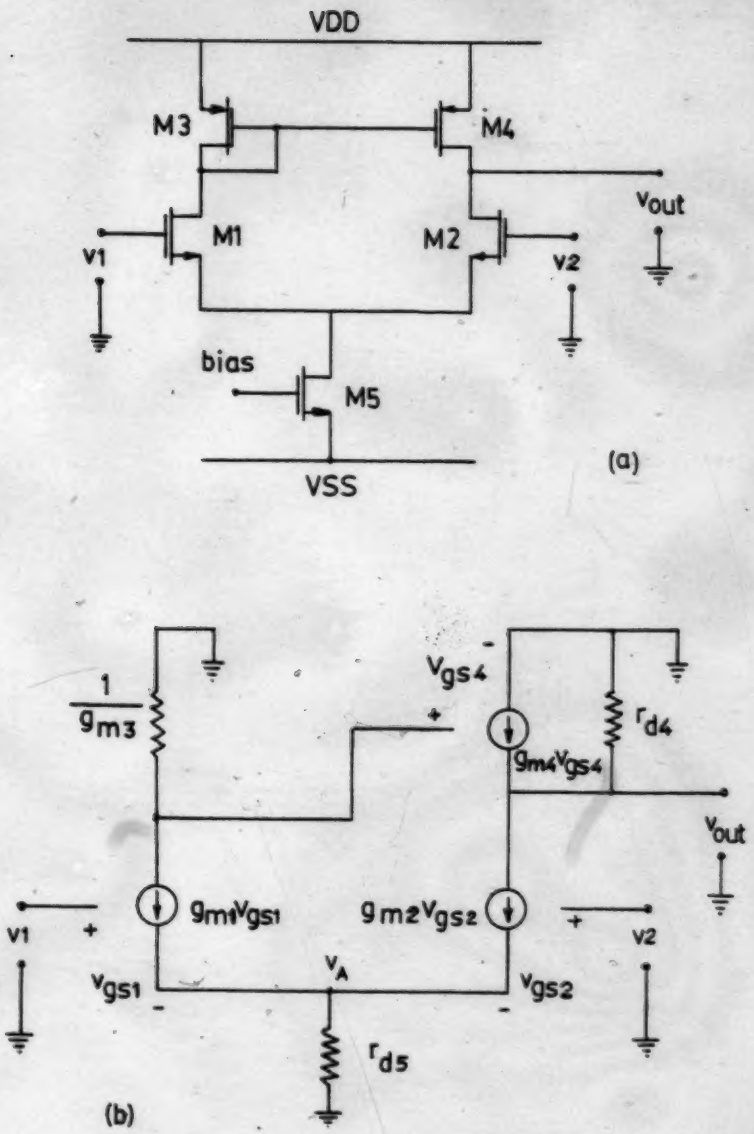


Figure 2.12 (a) A practical MOS differential stage (b) Its simplified equivalent circuit

$$CMRR = Adm / Acm \quad \text{.....(2.25)}$$

If we apply the assumptions made for equation (2.24) to equation (2.23), we get Acm = 0 and CMRR = ∞. This is the theoretical limit and is never achieved in practice because of body effect, finite drain-to-source resistance and device mismatch.

2.6 Frequency Compensation

Frequency compensation is used to guarantee stable operation of an Op-amp in feedback configurations with a closed loop gain of 1. In case of bipolar Op-amps this is generally done by connecting a capacitor between the output and input of an inverting stage. This capacitor will introduce a dominant pole at a low frequency so as to ensure a rolloff of 20 dB per decade in the open-loop frequency response till the unity-gain frequency.

To understand the effects of this compensation capacitor, consider figure 2.13(a). This shows the simplified small-signal equivalent circuit of a two-stage Op-amp. R_1 and C_1 represent the total resistance and capacitance of the first stage, and R_2 and C_2 represent the corresponding quantities for the second stage, including the load. This circuit has been studied by many authors[4,11,12], and assuming that the poles are widely spaced, the pole and zero location can be determined approximately as:

$$P1 \cong -1/[(1 + g_{m_2}R_2).Ck.R_1] \quad \text{.....(2.26)}$$

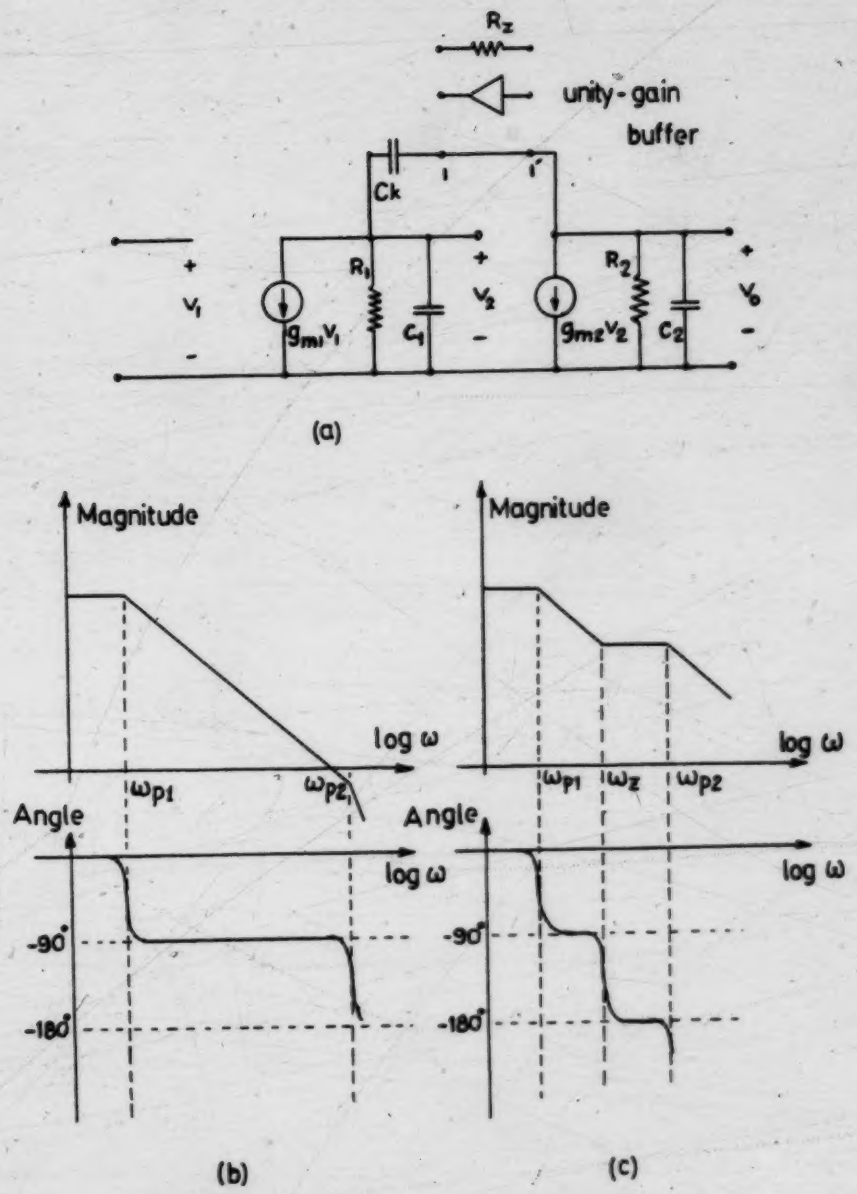


Figure 2.13 (a) Simplified equivalent circuit of a two-stage Op-amp (b) Frequency response of the amplifier for g_m large (c) Frequency response of the amplifier for g_m small

$$P2 \cong -g_{m2}.Ck \,/[C_1(C_2 + Ck) + Ck.C_2] \quad \ldots\ldots\ldots\ldots (2.27)$$

$$Z = + g_{m2} \,/\, Ck \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.28)$$

Note that the presence of Ck at the denominator of P1 pushes it to a very high frequency, while P2 is moved down to a lower frequency due to the Miller multiplication of the compensation capacitance Ck by the gain of the second stage. For this reason this compensation technique is often called 'pole-splitting'.

However, this simple technique in not entirely suitable for MOS Op-amps. This is due to the relatively low transconductance of MOS circuits as compared to bipolar circuits. The high transconductance of bipolar circuit pushes the right-half plane zero (see equation 2.28) to a value much higher than the unity-gain frequency, and therefore it can be neglected. But in MOS circuits the relatively low value of g_m reduces the zero considerably. The resulting frequency response of the MOS Op-amp is shown in figure 2.13(c). The zero reduces the phase by 90 degree, and at the same time prevents the magnitude from rolling off at the initial rate of 20 dB per decade. Therefore the phase exceeds 180 degree before the magnitude becomes 1, rendering the circuit unstable when connected in a unity-gain configuration.

This unique problem of MOS operational amplifiers can be eliminated in two ways. Because of the finite transconductance of the second stage, at high frequencies the signal can flow directly through the compensation

capacitor Ck to the output, causing a 180 degree phase inversion beyond a certain frequency. This is also called 'feed-forward' or 'signal feed-through'. The first method of compensation tries to eliminate signal feed-forward by putting a unity-gain buffer across points 1 - 1', as shown in figure 2.13(a). This buffer allows feedback, necessary for the Miller effect, but prevents feed-forward. In the second method instead of the unity gain buffer across the points 1 - 1' of figure 2.13(a), a resistor R_z, called 'nulling resistor', is connected. Assuming that R_z is much smaller than R_1 and R_2, and further assuming that the poles are reasonably wide spaced, it can be shown[11] that the poles remain the same as given by equations 2.26 and 2.27, while the zero is given by

$$Z' = [Ck.(1/g_{m2} - R_z)]^{-1} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.29)$$

From the above equation we can see that if R_z is made equal to $1/g_{m2}$, the zero vanishes. This is the design criteria for selecting the value of R_z.

Another important factor to be kept in mind while designing an Op-amp is the effect of capacitive loading on the frequency response. To investigate this, consider the non-dominant pole given by the equation 2.27. In case of large capacitive loading we may take $C_2.Ck >> C_1(C_2 + Ck)$. With this assumption; equation 2.27 can be approximated as

$$P_2 \cong -g_{m2}Ck \,/\, (C_2Ck) = -g_{m2}/C_2 \quad \ldots\ldots\ldots\ldots\ldots (2.30)$$

Thus the non-dominant pole is located at a frequency given by $-g_{m2}/C_2$. The unity cross-over frequency of the Op-amp can

be approximated as g_{m1}/Ck, so that in order to insure that the phase margin is not greatly degraded by the presence of the capacitive loading, we must make sure that

$$(g_{m2}/C_2) >> (g_{m1}/Ck) \quad \text{.....(2.31)}$$

If we make g_{m2} to be larger than g_{m1} by a factor of about two to five, then it is generally possible to drive a capacitive load on the same order of magnitude as the compensating capacitor. For larger loads an output stage may be required.

2.7 Steps for designing Op-amps

The general steps involved in desinging an Op-amp is outlined below. These steps are followed in the design of each of the three Op-amps described in chapter 3.

1. Choose the circuit. There are a number of circuits reported in the literature. The one that meets most of the required performance criteria may be chosen for further investigation.
2. Select suitable voltages and currents. Calculate the size of each device using equation (3.1). See also section 3.1.
3. Do the dc analysis using SPICE[8].
4. Repeat steps 2 and 3 till the required bias is established.
5. Do the ac small singal analysis using SPICE.
6. Change voltages, currents and device sizes, and repeat step 5 till the required ac small signal performance is

obtained. More details may be found in chapters 2 and 3.

7. Prepare layout according to the design rules[13], and send it for fabrication.
8. The testing procedure for the fabricated chip is outlined in chapter 5.

3. DESIGN OF THE OP-AMPS

This chapter describes the design and performance analysis (using SPICE) of three CMOS Op-amps. All the Op-amps have been fabricated using the Northern Telecom CMOS-1B process and the results of different tests on the fabricated chip are discussed in chapter 6. There is a good agreement between the simulated and actual results.

3.1 OP-AMP # 1

As this is the first of the three Op-amps described in this thesis, it is hereafter called Op-amp # 1. Figure 3.1 shows the circuit diagram. Transistors M8 (diode-connected), M5 and M7 form simple current sources for biasing the differential input stage and the gain stage. Transistors M1 through M5 form the differential input stage and transistors M6 and M7 form the gain stage. Capacitor Ck is used for frequency compensation. Diode-connected transistor M9 acts as a resistor to establish the bias current through transistor M8.

3.1.1 Design of the circuit

There are two phases in the design cycle - hand calculations and SPICE simulation. It may be required to repeat this cycle several times before arriving at a final design.

The most useful design equation is equation (2.1), which is rewritten here in a modified form :

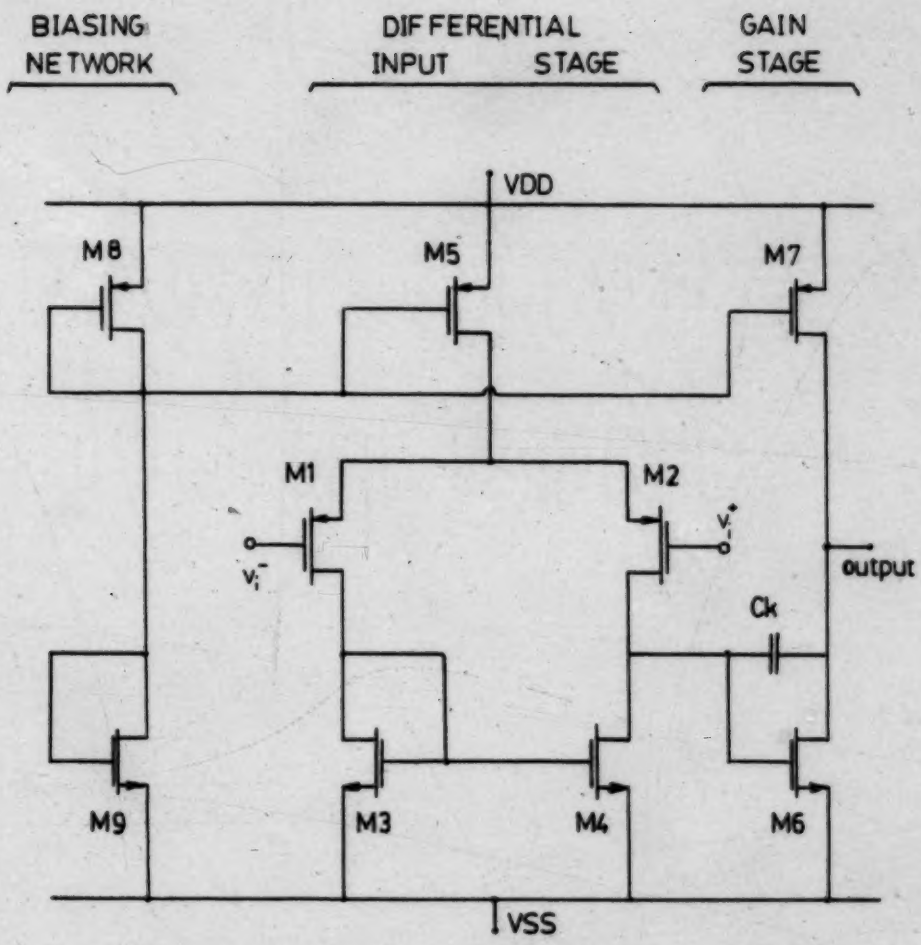


Figure 3.1 Circuit diagram of Op-amp # 1

$$ID = k'(W/L)(VGS-VTH)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

where $k'=(\mu C_{ox})/2$. For hand calculations of those designs that are to be fabricated using Northern Telecom CMOS-1B process, k' may be taken as $4.5\mu A/V^2$ for p-channel MOSFETs, and $10\mu A/V^2$ for n-channel MOSFETs. Although the minimum dimension in NT CMOS-1B process is about 6 microns, we take the minimum length of any device as 10 micron as there is a better agreement between calculated and simulated results for lengths greater than 10 microns.

The next step in the design is to decide the currents through each stage of the circuit. Generally the drain current in each of the input devices of a differential stage would be in the range of 5 to 25μA. Drain current in the second stage will be about 5 to 10 times higher than that in the differential stage. While low current levels increase the gain of the transistor, higher speed is obtained with higher bias currents. Keeping this in mind, we choose ID=10μA in the differential stage, and ID=100μA in the gain stage. For the biasing network ID is selected as 30μA. With this we can proceed to find the W/L ratio for each transistor.

(a) Transistors M3 and M4

For the sake of simplicity, assume W=L=10 microns. The drain current has been chosen to be 10 μA. Therefore

$$10\mu A = 10\mu(1)(VGS-VTH)^2$$

or

$$VGS = 1.95\ V$$

so for M3 and M4 : W/L = 10/10

(b) Transistor M5

Drain current = (10+10)μA = 20μA

Assume VGS = 1.95 V, and let L=10 microns

From (3.1),

$$20\mu A = 4.5\ \mu(W/10)(1.95-0.95)^2$$

or, W = 200/4.5 = 44.45

So for M5 : W/L = 44.45/10 $\cong$ 44.5/10

(c) Transistors M1 and M2

Assume VGS to be 2.2 V

Drain current is 10μA

As the source potential is not the same as that of the substrate, the threshold voltage changes. Assuming a VSB of 2V, from figure 2.10, we may take VTH approximately as 1.55V.

Then, using (3.1),

$$W/L = 10\mu A/\ 4.5\mu(2.2-1.55)^2 \cong 10/1.9$$

choose W/L as 60/12

(d) Transistor M6

Drain current through M6 and M7 is assumed as 100μA. VGS from calculations for M5 is 1.95 V. So from (3.1),

$$W/L = 100\ \mu A\ /10\mu(1.95-0.95)^2$$

or W/L = 100/10 for M6

(e) Transistor M7

Drain current is 100μA. Assuming VGS = VDS for transistor M4, VGS for M7 is 1.95 volts. So from (3.1),

$$W/L = 100\mu A\ /4.5\mu(1.95-0.95)^2$$

$= 100/4.5$

Multiply and divide by 10 to make L=10 microns.

Then W/L = 222/10 for M7.

(f) Transistor M8

Drain current has been assumed as 30μA. VGS is 1.95 V. For simplicity assume L=10 microns. Then, from (3.1),

$$30\mu A = 4.5\mu(W/10)(1.95-0.95)^2$$

or $W = 300/4.5 \cong 66.67$

So for M8 choose W/L = 66.7/10

(g) Transistor M9

ID = 30μA. Assuming VDD = +5 V, and VSS = -5 V, VGS=VDS=8.05 V. To drop 8.05 volts, the width should be small and the length should be large. Assume a reasonable value of 8 microns for width. Then from (3.1),

$$30\mu A = 10\ \mu(8/L)(8.05-0.95)^2$$

or $$L = 8/3\ (7.1)^2$$

$$L = 134.4 \text{ microns}$$

for M9, W/L = 8/134.4

3.1.2 Simulation using SPICE

The next step after the initial hand design is to find out the operating points using SPICE. There will be small deviations in currents and voltages with respect to the values obtained from hand calculations. Small changes in the values of voltages and currents can be accepted, except at the output. When the two inputs are held at ground potential, the dc voltage at the output should be zero. If

this is not zero, appropriate changes should be made to the W values such that the output dc voltage is very nearly equal to zero.

After this we can use the other circuit analysis facilities provided by SPICE like ac analysis, transient analysis, etc., to arrive at a good design.

For a complete description of SPICE, see reference [8].

3.1.2.1 DC operating point determination using SPICE

Figure 3.2 shows the node assignment used for SPICE simulation program. The SPICE program for calculating the operating point is listed below, with appropriate comments :

```
OP-AMP #1
*
*  Select appropriate options from
*  .OPTIONS card
*
.OPTIONS ABSTOL=1N VNTOL=1U NUMDGT=4 CPTIME=5
*
.WIDTH IN=80 OUT=70
*
*  Use .MODEL card to describe the NT CMOS-1B process
*  First NMOS, then PMOS
*
.MODEL NTNMOS NMOS(LEVEL=2 VTO=1.0 PB=0.7
+  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
+  RSH=15.0        CJ=4.0E-4       MJ=2.0
+  CJSW=8.0E-10    MJSW=2.0        JS=1.0E-6
+  TOX=8.5E-8      NSUB=1.0E16     XJ=1.0E-6
+  LD=0.7E-6       UO=750          UCRIT=5.0E4
+  UEXP=0.14       VMAX=5.0E4)
*
*
.MODEL NTPMOS PMOS(LEVEL=2 VTO=-1.0 PB=0.7
+  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
+  RSH=75.0        CJ=1.8E-4       MJ=2.0
+  CJSW=6.0E-10    MJSW=2.0        JS=1.0E-6
+  TOX=8.5E-8      NSUB=2.0E15     XJ=0.9E-6
+  LD=0.6E-6       UO=250          UCRIT=1.0E4
```

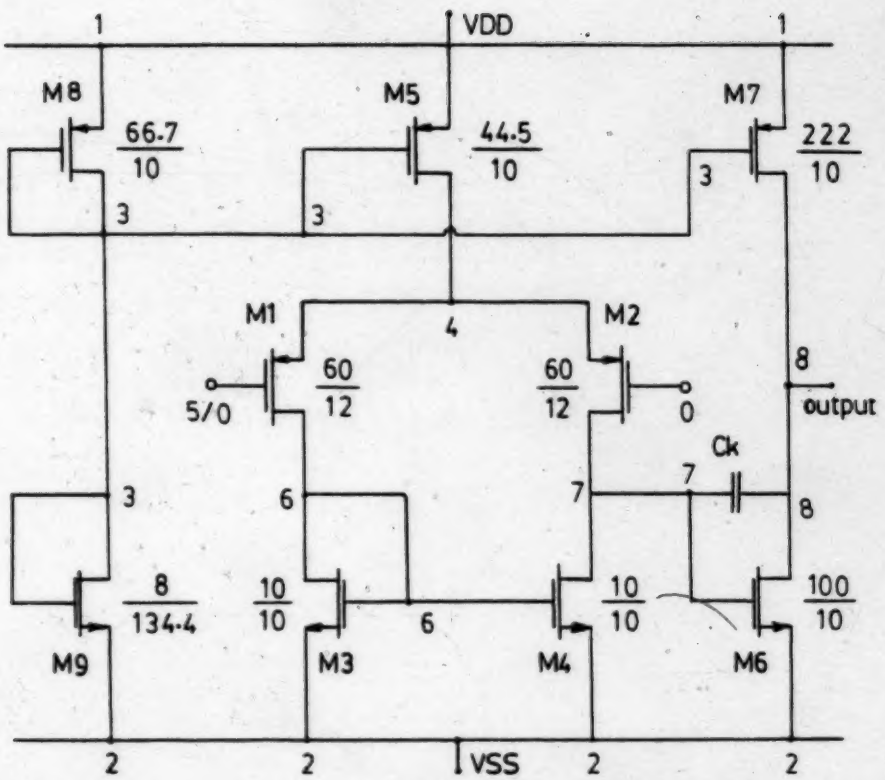


Figure 3.2 Node assignments and W/L values for simulation using SPICE of Op-amp # 1

```
+  UEXP=0.03      VMAX=3.0E4)
*
*  Circuit description (refer to figure 3.2)
*  Other parameters like AD, AS,...are not given now)
*
M1   6   0   4   1   NTPMOS  W=60U    L=12U
M2   7   0   4   1   NTPMOS  W=60U    L=12U
M3   6   6   2   2   NTNMOS  W=10U    L=10U
M4   7   6   2   2   NTNMOS  W=10U    L=10U
M5   4   3   1   1   NTPMOS  W=44.5U  L=10U
M6   8   7   2   2   NTNMOS  W=100U   L=10U
M7   8   3   1   1   NTPMOS  W=222.0U   L=10U
M8   3   3   1   1   NTPMOS  W=66.7U  L=10U
M9   3   3   2   2   NTNMOS  W=8U     L=134.4U
*
*  Supply and measuring voltages
*
VDD  1   0   DC  5
VSS  0   2   DC  5
*
*  Compensating capacitor (use an appropriate
*  value like 5pF to start with)
*
CK   7   8   5PF
*
*  Include the desired load here
*
*
*  Perform dc analysis
*
.OP
*
*  Perform other analysis, and print/plot the results
*
*
*
.END
```

The results of this simulation are :

```
1***12-22-84 ***  SPICE 2G.5A (23NOV82) ***04:22:32***

0OP-AMP #1

0***     INPUT LISTING     TEMPERATURE =  27.000 DEG C

0**************************************************************


 *
 *  Select appropriate options from
 *  .OPTIONS card
 *
 .OPTIONS ABSTOL=1N VNTOL=1U NUMDGT=4 CPTIME=5
 *
 .WIDTH IN=80 OUT=70
 *
 *  Use .MODEL card to describe the NT CMOS-1B process
 *  First NMOS, then PMOS
 *
 .MODEL NTNMOS NMOS(LEVEL=2 VTO=1.0 PB=0.7
 +  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
 +  RSH=15.0        CJ=4.0E-4       MJ=2.0
 +  CJSW=8.0E-10    MJSW=2.0        JS=1.0E-6
 +  TOX=8.5E-8      NSUB=1.0E16     XJ=1.0E-6
 +  LD=0.7E-6       UO=750          UCRIT=5.0E4
 +  UEXP=0.14       VMAX=5.0E4)
 *
 *
 .MODEL NTPMOS PMOS(LEVEL=2 VTO=-1.0 PB=0.7
 +  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
 +  RSH=75.0        CJ=1.8E-4       MJ=2.0
 +  CJSW=6.0E-10    MJSW=2.0        JS=1.0E-6
 +  TOX=8.5E-8      NSUB=2.0E15     XJ=0.9E-6
 +  LD=0.6E-6       UO=250          UCRIT=1.0E4
 +  UEXP=0.03       VMAX=3.0E4)
 *
 *  Circuit description (refer to figure 3.2)
 *  Other parameters like AD, AS,...are not given now)
 *
 M1   6   0   4   1   NTPMOS   W=60U    L=12U
 M2   7   0   4   1   NTPMOS   W=60U    L=12U
 M3   6   6   2   2   NTNMOS   W=10U    L=10U
 M4   7   6   2   2   NTNMOS   W=10U    L=10U
 M5   4   3   1   1   NTPMOS   W=44.5U  L=10U
 M6   8   7   2   2   NTNMOS   W=100U   L=10U
 M7   8   3   1   1   NTPMOS   W=222.0U    L=10U
 M8   3   3   1   1   NTPMOS   W=66.7U  L=10U
 M9   3   3   2   2   NTNMOS   W=8U     L=134.4U
 *
```

```
*  Supply and measuring voltages
*
VDD  1  0  DC  5
VSS  0  2  DC  5
*
*  Compensating capacitor (use an appropriate
*  value like 5pF to start with)
*
CK  7  8  5PF
*
*  Include the desired load here
*
*
*  Perform dc analysis
*
.OP
*
*  Perform other analysis, and print/plot the results
*
*
*
.END
```

```
1***12-22-84 *** SPICE 2G.5A (23NOV82) ***04:22:32****

0OP-AMP #1

0* MOSFET MODEL PARAMETERS  TEMPERATURE = 27.000 DEG C

0*************************************************************
```

	NTNMOS	NTPMOS
0TYPE	NMOS	PMOS
0LEVEL	2.000	2.000
0VTO	1.000	-1.000
0KP	3.05E-05	1.02E-05
0GAMMA	1.418	0.634
0PHI	0.695	0.612
0PB	0.700	0.700
0CGSO	4.00E-10	4.00E-10
0CGDO	4.00E-10	4.00E-10
0CGBO	2.00E-10	2.00E-10
0RSH	15.000	75.000
0CJ	4.00E-04	1.80E-04
0MJ	2.000	2.000
0CJSW	8.00E-10	6.00E-10
0MJSW	2.000	2.000
0JS	1.00E-06	1.00E-06
0TOX	8.50E-08	8.50E-08
0NSUB	1.00E+16	2.00E+15
0TPG	1.000	1.000
0XJ	1.00E-06	9.00E-07
0LD	7.00E-07	6.00E-07

```
0UO             750.000    250.000
0UCRIT         5.00E+04   1.00E+04
0UEXP             0.140      0.030
0VMAX          5.00E+04   3.00E+04


1****12-22-84 *** SPICE 2G.5A (23NOV82) ***04:22:32****

0OP-AMP #1

0* SMALL SIGNAL BIAS SOLUTION  TEMPERATURE = 27.0 DEG C

0**********************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)   -5.0000    (  3)    3.1335

(  4)    2.1173    (  6)   -3.1568    (  7)   -3.1568

(  8)   -0.3185


     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD       -1.321E-04

     VSS       -1.321E-04

     TOTAL POWER DISSIPATION   1.32E-03  WATTS
```

```
1***12-22-84 **** SPICE 2G.5A (23NOV82) ****04:22:32***

0OP-AMP #1

0* OPERATING POINT INFORMATION TEMPERATURE = 27.0 DEG C

**************************************************************

0
0**** MOSFETS

```

0MODEL	M1 NTPMOS	M2 NTPMOS	M3 NTNMOS	M4 NTNMOS	M5 NTPMOS
ID	-8.51E-06	-8.51E-06	8.51E-06	8.51E-06	-1.70E-05
VGS	-2.117	-2.117	1.843	1.843	-1.866
VDS	-5.274	-5.274	1.843	1.843	-2.883
VBS	2.883	2.883	0.0	0.0	0.0
VTH	-1.562	-1.562	0.950	0.950	-0.959
VDSAT	-0.475	-0.475	0.501	0.501	-0.674
GM	3.01E-05	3.01E-05	1.93E-05	1.93E-05	3.71E-05
GDS	2.55E-07	2.55E-07	2.74E-07	2.74E-07	6.82E-07
GMB	4.14E-06	4.14E-06	1.32E-05	1.32E-05	1.06E-05
CBD	0.0	0.0	0.0	0.0	0.0
CBS	0.0	0.0	0.0	0.0	0.0
CGSOVL	2.40E-14	2.40E-14	4.00E-15	4.00E-15	1.78E-14
CGDOVL	2.40E-14	2.40E-14	4.00E-15	4.00E-15	1.78E-14
CGBOVL	2.16E-15	2.16E-15	1.72E-15	1.72E-15	1.76E-15
CGS	1.76E-13	1.76E-13	2.33E-14	2.33E-14	1.06E-13
CGD	0.0	0.0	0.0	0.0	0.0
CGB	-4.93E-32	-4.93E-32	0.0	0.0	0.0

0MODEL	M6 NTNMOS	M7 NTPMOS	M8 NTPMOS	M9 NTNMOS
ID	9.08E-05	-9.08E-05	-2.43E-05	2.43E-05
VGS	1.843	-1.866	-1.866	8.134
VDS	4.681	-5.319	-1.866	8.134
VBS	0.0	0.0	0.0	0.0
VTH	0.939	-0.955	-0.963	0.996
VDSAT	0.508	-0.675	-0.670	4.842
GM	2.04E-04	1.99E-04	5.31E-05	6.67E-06
GDS	1.76E-06	2.72E-06	1.23E-06	2.03E-08
GMB	1.38E-04	5.61E-05	1.53E-05	2.73E-06
CBD	0.0	0.0	0.0	0.0
CBS	0.0	0.0	0.0	0.0
CGSOVL	4.00E-14	8.88E-14	2.67E-14	3.20E-15
CGDOVL	4.00E-14	8.88E-14	2.67E-14	3.20E-15
CGBOVL	1.72E-15	1.76E-15	1.76E-15	2.66E-14
CGS	2.33E-13	5.29E-13	1.59E-13	2.88E-13
CGD	-7.89E-31	0.0	0.0	-2.96E-31
CGB	0.0	0.0	0.0	0.0

```
JOB CONCLUDED
TOTAL JOB TIME            0.0
```

Table 3.1 gives the value of drain current and gate-to-source voltage for each transistor. Both the assumed (or hand-calculated) and simulation results are given side-by-side for comparison. Although there is some difference, it is not serious. The purpose of hand-calculation is to give a good feeling for the circuit, and some suitable starting values for simulation. The simulation results should be taken as the accurate results.

Also from the results we can note that the dc output voltage when the input to both the input transistors (M1 and M2) is zero is about 0.3185 volts. This means there is a built-in offset voltage. This can be avoided by varying the width of transistor M7 (or M6). By repeated trails it was found that for a value of (W/L) of M7 = 225.6/10 the dc output voltage is +2.6mV. This value of W/L (namely W/L = 225.6/10) is taken as final value unless we choose to change it in the sections to come.

3.1.2.2 AC analysis using SPICE

SPICE can be used to study the AC small-signal characteristics of an Op-amp. While studying the small-signal characteristics, it is important to make sure that the dc voltage of the output is around zero when both the inputs are tied to the ground. If this is not the case, and if the dc output is slightly below the positive or negative supply voltages, the ac analysis can be grossly inaccurate.

Table 3.1 Hand-calculation and first simulation results tabulated for Op-amp # 1

DEVICE	W,L Microns	HAND CALCULATION			FIRST SIMULATION RUN		
		|VGS| Volts	|VTH| Volts	|ID| uA	|VGS| Volts	|VTH| Volts	|ID| uA
M1	60,12	2.2	1.55	10	2.117	1.562	8.51
M2	60,12	2.2	1.55	10	2.117	1.562	8.51
M3	10,10	1.95	0.95	10	1.843	0.95	8.51
M4	10,10	1.95	0.95	10	1.843	0.95	8.51
M5	44.5,10	1.95	0.95	20	1.866	0.959	17.0
M6	100,10	1.95	0.95	100	1.843	0.939	90.8
M7	222,10	1.95	0.95	100	1.866	0.955	90.8
M8	66.7,10	1.95	0.95	30	1.866	0.963	24.3
M9	8,134.4	8.05	0.95	30	8.134	0.996	24.3

The ac small-signal gain, input resistance, output resistance, and the frequency response of the Op-amp described in section 3.1.2 can be obtained by including the following lines with the program given in section 3.1.3.1 :

```
*  ac input voltage
VIN  5  0   AC  0.001
*
*    load resistance and capacitance
*
RL  8  0  5MEG
CL  8  0  15PF
*
*    ac  analysis
*
.TF  V(8)  VIN
.AC  DEC  8  1  10MEG
.PRINT AC VM(8) VP(8)
*    VM(8) is the magnitude of the ac
*    voltage at node 8, and VP(8) is
*    its phase.
.PLOT  AC  V(8)
```

The results of this piece of program are given below:

```
0****     SMALL-SIGNAL CHARACTERISTICS

0  V(8)/VIN                              = -2.479E+03
0  INPUT RESISTANCE AT VIN          =  1.000E+20
0  OUTPUT RESISTANCE AT V(8)        =  2.155E+05


1**12-22-84 ****  SPICE 2G.5A (23NOV82) ****03:58:54***

0OP-AMP #1

0**  AC ANALYSIS   TEMPERATURE =   27.000 DEG C

0*************************************************************

     FREQ       VM(8)       VP(8)
X

  1.000E+00     2.479E+00   1.798E+02
  1.334E+00     2.479E+00   1.798E+02
  1.778E+00     2.479E+00   1.797E+02
  2.371E+00     2.479E+00   1.796E+02
```

3.162E+00	2.478E+00	1.795E+02
4.217E+00	2.478E+00	1.793E+02
5.623E+00	2.478E+00	1.791E+02
7.499E+00	2.478E+00	1.788E+02
1.000E+01	2.478E+00	1.784E+02
1.334E+01	2.477E+00	1.779E+02
1.778E+01	2.476E+00	1.772E+02
2.371E+01	2.473E+00	1.763E+02
3.162E+01	2.469E+00	1.750E+02
4.217E+01	2.462E+00	1.734E+02
5.623E+01	2.450E+00	1.712E+02
7.499E+01	2.428E+00	1.684E+02
1.000E+02	2.390E+00	1.647E+02
1.334E+02	2.328E+00	1.599E+02
1.778E+02	2.228E+00	1.540E+02
2.371E+02	2.078E+00	1.469E+02
3.162E+02	1.872E+00	1.391E+02
4.217E+02	1.621E+00	1.308E+02
5.623E+02	1.348E+00	1.229E+02
7.499E+02	1.084E+00	1.159E+02
1.000E+03	8.490E-01	1.100E+02
1.334E+03	6.536E-01	1.052E+02
1.778E+03	4.978E-01	1.015E+02
2.371E+03	3.766E-01	9.865E+01
3.162E+03	2.839E-01	9.645E+01
4.217E+03	2.135E-01	9.478E+01
5.623E+03	1.604E-01	9.349E+01
7.499E+03	1.204E-01	9.249E+01
1.000E+04	9.030E-02	9.170E+01
1.334E+04	6.774E-02	9.105E+01
1.778E+04	5.080E-02	9.049E+01
2.371E+04	3.810E-02	8.997E+01
3.162E+04	2.857E-02	8.944E+01
4.217E+04	2.142E-02	8.887E+01
5.623E+04	1.606E-02	8.821E+01
7.499E+04	1.204E-02	8.739E+01
1.000E+05	9.026E-03	8.636E+01
1.334E+05	6.763E-03	8.503E+01
1.778E+05	5.063E-03	8.328E+01
2.371E+05	3.786E-03	8.099E+01
3.162E+05	2.826E-03	7.796E+01
4.217E+05	2.101E-03	7.399E+01
5.623E+05	1.552E-03	6.880E+01
7.499E+05	1.135E-03	6.210E+01
1.000E+06	8.173E-04	5.366E+01
1.334E+06	5.750E-04	4.332E+01
1.778E+06	3.930E-04	3.119E+01
2.371E+06	2.607E-04	1.759E+01
3.162E+06	1.690E-04	2.991E+00
4.217E+06	1.085E-04	-1.216E+01
5.623E+06	7.011E-05	-2.744E+01
7.499E+06	4.618E-05	-4.242E+01
1.000E+07	3.110E-05	-5.669E+01

```
********02-03-85 ********  SPICE 3B.5A (23NOV82) *********21:54:44******

OP-AMP #1

****     AC ANALYSIS                    TEMPERATURE =   27.000 DEG C

******************************************************************************

X
    FREQ       V(8)
X                    1.000E-06     1.000E-04     1.000E-02     1.000E+00  1.000E+02
 1.000E+00  2.479E+00 .                                                    .
 1.334E+00  2.479E+00 .                                                    .
 1.778E+00  2.479E+00 .                                                    .
 2.371E+00  2.479E+00 .                                                    .
 3.162E+00  2.478E+00 .                                                    .
 4.217E+00  2.478E+00 .                                                    .
 5.623E+00  2.478E+00 .                                                    .
 7.499E+00  2.478E+00 .                                                    .
 1.000E+01  2.478E+00 .                                                    .
 1.334E+01  2.477E+00 .                                                    .
 1.778E+01  2.476E+00 .                                                    .
 2.371E+01  2.473E+00 .                                                    .
 3.162E+01  2.469E+00 .                                                    .
 4.217E+01  2.462E+00 .                                                    .
 5.623E+01  2.450E+00 .                                                    .
 7.499E+01  2.428E+00 .                                                    .
 1.000E+02  2.390E+00 .                                                    .
 1.334E+02  2.328E+00 .                                                    .
 1.778E+02  2.228E+00 .                                                    .
 2.371E+02  2.078E+00 .                                                    .
 3.162E+02  1.872E+00 .                                                    .
 4.217E+02  1.621E+00 .                                                    .
 5.623E+02  1.348E+00 .                                                    .
 7.499E+02  1.084E+00 .                                                    .
 1.000E+03  8.490E-01 .                                                    .
 1.334E+03  6.536E-01 .                                                    .
 1.778E+03  4.978E-01 .                                                    .
 2.371E+03  3.766E-01 .                                                    .
 3.162E+03  2.839E-01 .                                                    .
 4.217E+03  2.135E-01 .                                                    .
 5.623E+03  1.604E-01 .                                                    .
 7.499E+03  1.204E-01 .                                                    .
 1.000E+04  9.030E-02 .                                                    .
 1.334E+04  6.774E-02 .                                                    .
 1.778E+04  5.080E-02 .                                                    .
 2.371E+04  3.810E-02 .                                                    .
 3.162E+04  2.857E-02 .                                                    .
 4.217E+04  2.142E-02 .                                                    .
 5.623E+04  1.606E-02 .                                                    .
 7.499E+04  1.204E-02 .                                                    .
 1.000E+05  9.026E-03 .                                                    .
 1.334E+05  6.763E-03 .                                                    .
 1.778E+05  5.063E-03 .                                                    .
 2.371E+05  3.786E-03 .                                                    .
 3.162E+05  2.826E-03 .                                                    .
 4.217E+05  2.101E-03 .                                                    .
 5.623E+05  1.552E-03 .                                                    .
 7.499E+05  1.135E-03 .                                                    .
 1.000E+06  8.173E-04 .                                                    .
 1.334E+06  5.750E-04 .                                                    .
 1.778E+06  3.930E-04 .                                                    .
 2.371E+06  2.607E-04 .                                                    .
 3.162E+06  1.690E-04 .                                                    .
 4.217E+06  1.085E-04 .                                                    .
 5.623E+06  7.011E-05 .                                                    .
 7.499E+06  4.618E-05 .                                                    .
 1.000E+07  3.110E-05 .                                                    .

Y

      JOB CONCLUDED

      TOTAL JOB TIME            0.0
```

From the results we see that the circuit has an ac small-signal gain of about 2479; very high input resistance, and high output resistance. Also the unity-gain frequency is about 750 to 800 KHz, which is relatively low.

Once we know how to get all these results, we can try different combinations of W/L's, drain currents, and compensation capacitor values to arrive at a satisfactory value of W/L values for each transistor.

3.1.3 Final selection of W/L values

After trying a lot of different combinations it was found that the set of values shown in table 3.2 provide a reasonably good performance. Comparing these values with that given in table 3.1, we see that the output transistors M6 and M7 have been made wider, resulting in increased drain currents for the second stage. This helps in providing some additional gain, but the unity-gain frequency remains almost unchanged. Also the capacitance value has been cut from 5 pF to 4.2 pF. This helps in saving some silicon real estate.

3.1.4 Layout Preparation

All the Op-amp circuits given in this thesis were fabricated by Northern Telecom Electronics, Ottawa, using their CMOS-1B process. For a description of Northern Telecom CMOS-1B process and the associated design rules see reference [13].

Table 3.2 Final width and length values for Op-amp # 1

DEVICE	WIDTH Microns	LENGTH Microns
M1	60	12
M2	60	12
M3	10	10
M4	10	10
M5	44.5	10
M6	140	10
M7	320	10
M8	66.7	10
M9	8	134.4
CK : 4.2pF		

The layout of a particular circuit can, sometimes, greatly affect the circuit performance. There are no rigid rules that govern the layout and how it affects the performance of a circuit. Experience and familiarity help. For a novice, the best way is to have the layout almost similar to the circuit itself (and hope for the best!).

Layouts can be prepared using a CAD system, or manually, using a large graph sheet. We followed the latter method. It took careful planning and quite some time to come up with an acceptable layout that met all the design rules.

3.1.4.1 Compensation capacitor calculations

From reference [7], poly-to-poly capacitance is about (3.1±0.2)E-8 F/cm². If we take the worst case capacitance as 2.9E-8 F/cm², and we require a capacity of 4.2 pF, then we need an area of

$$[(4.2E\text{-}12X1)/(2.9E\text{-}8)]cm^2.$$

$$= 14482.759 \text{ sq.microns.}$$

Taking the length as 129 microns,

Width = (14482.759)/(129) = 112.3 microns

≅ 112 microns.

3.1.4.2 Layout in AHF language

The co-ordinates of the layout thus prepared on a big graph-paper were fed to a computer using the language AHF (Alberta High-level Form, developed at the University of Alberta). A detailed description of AHF language can be

found in reference [10]. The complete AHF program for the layout is listed in Appendix A.

Once we have the layout coded in AHF language, plots of the layout can be generated using computers. One such CALCOMP plot is attached in Appendix A. Also graphic terminals can be used to blow-up different parts of the layout to visually inspect the layout for any errors.

After carefully studying the layout and making sure that everything is correct, the AHF program can be converted to the standard CIF (Caltech Intermediate Form), which can be sent to Northern Telecom for fabrication.

3.1.5 Final Simulation Results

After preparing the layout drain area, source area, perimeter of drain, perimeter of source, number of squares in drain, and number of squares in source can be measured from the graph-sheet and entered in the SPICE program for an accurate analysis. Table 3.3 summarizes the final simulation results for Op-amp # 1.

3.1.6 Design Observations

At the time of writing this thesis, by which time the three Op-amps had been designed, we were able to observe some shortcomings of our very first Op-amp design. In the design section, for transistors M3 and M4, we had assumed a W/L of 10/10 for the sake of simplicity. But by increasing the width and the length we can increase the total gain of

Table 3.3 Final simulation results for Op-amp # 1

DEVICE	|ID| uA	|VGS| Volts	|VDS| Volts	|VTH| Volts
M1	8.5	2.117	5.274	1.562
M2	8.5	2.117	5.274	1.562
M3	8.5	1.843	1.843	0.95
M4	8.5	1.843	1.843	0.95
M5	17	1.865	2.883	0.959
M6	129	1.843	5.474	0.936
M7	130	1.865	4.526	0.955
M8	24.3	1.865	1.865	0.962
M9	24.3	8.135	8.135	0.996

DC Open-Loop Gain : 2457(67.8dB)
Unity Gain Frequency : 800 KHz
Supply Current IDD : 171 uA
Supply Current ISS : 171 uA
Power Dissipation : 1.71 mW
Die Area : 0.33 sq.mm (513 sq.mils)

the circuit slightly. Thus simply changing 10/10 to 20/20 would have provided an overall gain of 2831 instead of 2479. This would be preferred to increasing the current level of the second stage (which increases the power consumption). Also we never studied the step response, which is an important test to determine the performance of an Op-amp. Other than this, it is really thrilling to know that the fabricated Op-amp # 1 works 'the first-time'! The results obtained from the fabricated chip are discussed in chapter 6.

3.2 OP - AMP # 2

In this section the design and performance analysis of an Op-amp which has n-channel input transistors is described. Since this is the second Op-amp described in this thesis, it is hereafter called Op-amp # 2. The circuit diagram of Op-amp # 2 is shown in figure 3.3 This circuit consists of a differential gain stage, followed by a level-shifter, and a gain stage. Two transistors MB1 and MB2 establish the bias-current in the entire circuit.

3.2.1 Design of the circuit

In this design VDD is assumed to be +5 Volts, and VSS as -5 Volts. It is also assumed that all transistors (except the two transistors MC1 and MC2 in the compensation circuit) operate in the pinch-off region. Then the drain current is given by equation (2.1), which may be rewritten as

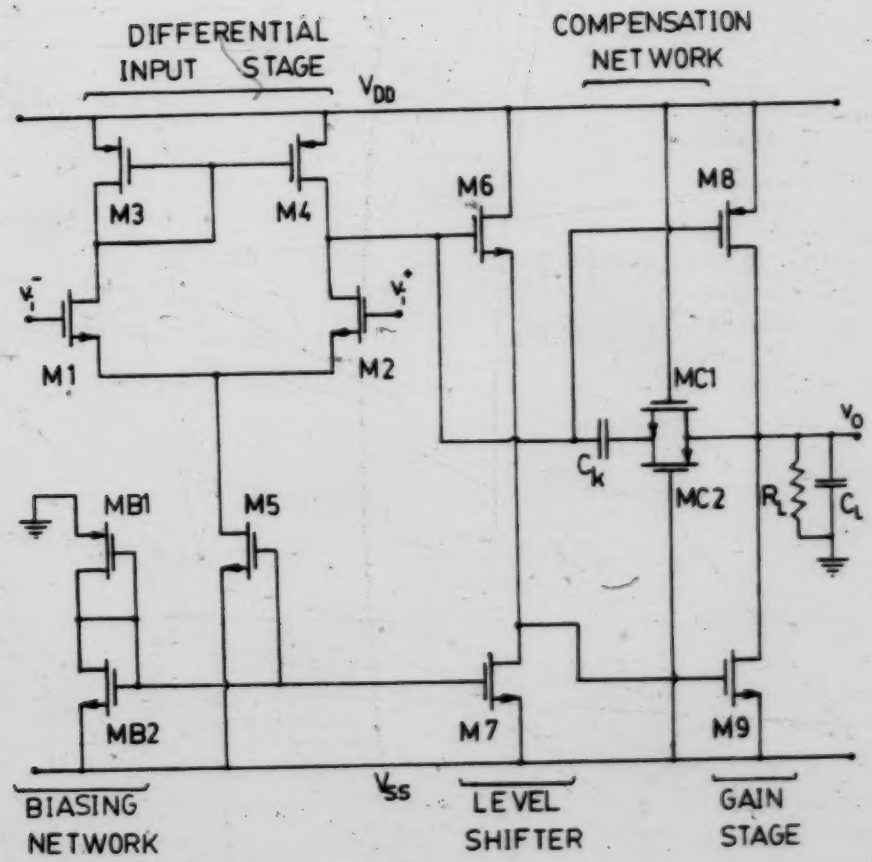


Figure 3.3 Circuit diagram of Op-amp # 2

$$(W/L) = ID/[k'(VGS-VTH)^2] \quad \ldots\ldots\ldots\ldots\ldots\ldots (3.2)$$

where

$$k' = (\mu C_{ox}/2) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.3)$$

The first step in the design is to choose appropriate currents through the different stages of the Op-amp circuit. As mentioned in the previous section, there is no precise way of choosing these currents. Only an approximate and appropriate guess is to be made. Let us select a current of 10μA through each of the input transistors, a current of 20μA through the level-shifter and a current of 60μA through the gain stage. To simplify the design, the current through the biasing network is also taken as 20μA. These current allotments are outlined in figure 3.4, which also shows the node allocation for SPICE simulation (discussed later).

The second step in the design is to choose the gate-to-source voltage drops. The choice of the gate-to-source voltage VGS is indicated for each transistor in the design part below:

(a) Transistors MB2, M5, and M7:

n-channel

Assume gate-to-source voltage = 2.1 volts

Drain current is 20μA

Threshold voltage is about 0.95 volts (source is tied to substrate)

k' for n-channel transistors is about 10 $\mu A/V^2$

So, using (3.2);

$$(W/L) = 20E\text{-}6/[10E\text{-}6(2.1\text{-}0.95)^2$$

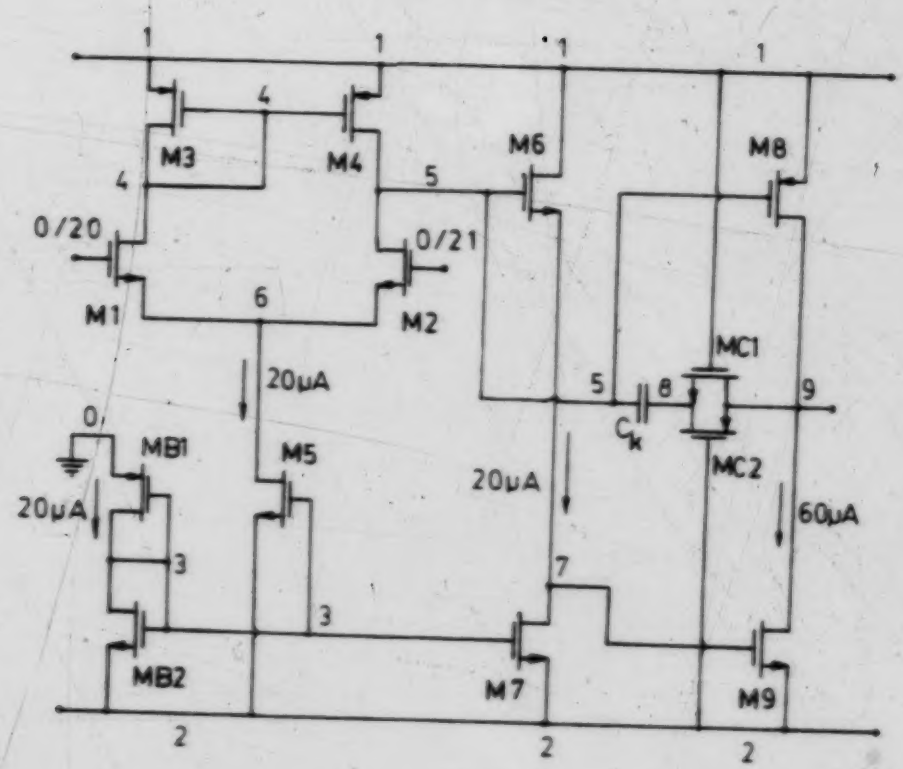


Figure 3.4 Op-amp # 2 : Initial current allotment for hand calculations, and node assignment for SPICE simulation

$= 2/(1.15)^2 \cong 1.51$

Select W=21 microns, L=14 microns.

(b) Transistors M3 and M4

p-channel

Assume gate-to-source voltage of 2.25 volts

Drain current is 10μA

Since the source is tied to substrate, threshold voltage is about 0.95 volts

k' for p-channel transistors is about 4.5 $\mu A/V^2$

Using (3.2);

$(W/L) = 10E\text{-}6/[4.5E\text{-}6(2.25\text{-}0.95)^2]$

$= 10/7.605 \cong 1.32$

Select W=50 microns, and L=38 microns.

(c) Transistors M1 and M2

n-channel

Assume gate-to-source voltage as 1.65 volts

Drain current is 10μA

Threshold voltage is about 0.95 volts, since the source is tied to the substrate.

Using (3.2)

$(W/L) = 10E\text{-}6/[10E\text{-}6(1.65\text{-}0.95)^2]$

$= 1/0.49 \cong 2.04$

Select W=51 microns, and L=25 microns

(d) Transistor MB1

p-channel

Gate-to-source voltage is 2.9 volts (since the gate-to-source / drain-to-source voltage of MB2 is assumed

to be 2.1 volts)

Drain current is 20μA

Threshold voltage is about 1.7 volts (since there is a source-to-substrate bias of 5 volts)

From equation (3.2),

$$(W/L) = 20E\text{-}6/[4.5E\text{-}6(2.9-1.7)^2]$$

$$\cong 20/6.48 \cong 30.86/10 \cong 31/10$$

Select W=31 microns, and L=10 microns.

(e) Transistor M6

n-channel

Gate-to-source voltage is

(10 - VDS of M4 - VDS of M7)

=(10 - 2.3 - 2.5) = 5.2 volts (Assuming VDS of M7 as 2.5 volts)

Drain current is 20μA

Threshold voltage is about 0.95 volts (source is tied to substrate)

Using equation (3.2)

$$(W/L) = 20E\text{-}6/[10E\text{-}6(5.2-0.95)^2]$$

$$\cong 2/18.1$$

Select W=8 microns, and L=72 microns.

(f) Transistor M8

p-channel

Gate-to-source voltage can be taken to be little over 2.25 volts (VGS of transistor M4); say 2.3 volts.

Drain current is 60μA

Threshold voltage is about 0.95 volts.

So from equation (3.2),

$$(W/L) = 60E\text{-}6/[4.5E\text{-}6(2.3-0.95)^2]$$

$$\cong 60/8.2 \cong 73/10$$

Select W=73 microns, L=10 microns.

(g) Transistor M9

n-channel

Gate-to-source voltage can be taken to be slightly above the VGS of M7 at about 2.5 volts

Drain current is 60μA

Threshold voltage is about 0.95 volts.

Then from equation (3.2),

$$(W/L) = 60E\text{-}6/[10E\text{-}6(2.5-0.95)^2]$$

$$\cong 6/2.4 \cong 25/10.$$

Choose W=25 microns, L=10 microns.

(h) Transistors MC1 and MC2

These two transistors together act as a resistor in series with the compensation capacitor. Their effective resistance should be approximately equal to $1/g_{m2}$ where g_{m2} is the transconductance of second or gain stage of figure 3.3. The method we have adopted to get an appropriate value of W/L for these transistors is as follows: First assume some reasonable value, say W/L = 15/15. Then carry out the dc analysis using SPICE, finding out g_m of the gain stage. Next, from the same dc analysis, find the effective resistance of MC1 in parallel with MC2. Modify W/L of MC1 and MC2 until satisfactory results are obtained.

Thus for the present, assume W/L = 15/15 for MC1 and MC2.

3.2.2 SPICE simulation

As a reminder we would like to mention that a detailed description of SPICE may be found in reference [8].

3.2.2.1 DC analysis

Figure 3.4 shows the circuit diagram of Op-amp # 2, and also the node assignment for SPICE simulation. Referring to the circuit diagram of figure 3.4 and using the W/L values derived in section 3.2.1, a SPICE program can be written to determine the dc operating points, in a manner similar to that of sections 3.1.3 and 3.1.3.1. The program is listed below:

```
OP-AMP # 2
*
*  Select appropriate options from
*  .OPTIONS card
*
.OPTIONS ABSTOL=1N VNTOL=1U NUMDGT=4 CPTIME=5
*
.WIDTH IN=80 OUT=70
*
*  Use .MODEL card to describe the NT CMOS-1B
*  process. First NMOS, then PMOS
*
.MODEL NTNMOS NMOS(LEVEL=2 VTO=1.0 PB=0.7
+  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
+  RSH=15.0        CJ=4.0E-4       MJ=2.0
+  CJSW=8.0E-10    MJSW=2.0        JS=1.0E-6
+  TOX=8.5E-8      NSUB=1.0E16     XJ=1.0E-6
+  LD=0.7E-6       UO=750          UCRIT=5.0E4
+  UEXP=0.14       VMAX=5.0E4)
*
*
.MODEL NTPMOS PMOS(LEVEL=2 VTO=-1.0 PB=0.7
```

```
+  CGSO=4.0E-10    CGDO=4.0E-10    CGBO=2.0E-10
+  RSH=75.0        CJ=1.8E-4       MJ=2.0
+  CJSW=6.0E-10    MJSW=2.0        JS=1.0E-6
+  TOX=8.5E-8      NSUB=2.0E15     XJ=0.9E-6
+  LD=0.6E-6       UO=250          UCRIT=1.0E4
+  UEXP=0.03       VMAX=3.0E4)
*
*  Circuit description (refer to figure 3.4)
*  AD and AS are approximate.
*
MB1 3 3 0 1 NTPMOS W=31U L=10U AD=100P AS=100P
MB2 3 3 2 2 NTNMOS W=21U L=14U AD=100P AS=100P
M1  4  0 6 6 NTNMOS W=51U L=25U AD=200P AS=200P
M2  5 0 6 6 NTNMOS W=51U L=25U AD=200P AS=200P
M3  4 4 1 1 NTPMOS W=50U L=38U AD=300P AS=300P
M4  5 4 1 1 NTPMOS W=50U L=38U AD=300P AS=300P
M5  6 3 2 2 NTNMOS W=21U L=14U AD=100P AS=100P
M6  1 5 7 7 NTNMOS W=8U L=72U AD=150P AS=150P
M7  7 3 2 2 NTNMOS W=21U L=14U AD=100P AS=100P
M8  9 5 1 1 NTPMOS W=73U L=10U AD=300P AS=300P
M9  9 7 2 2 NTNMOS W=25U L=10U AD=150P AS=150P
MC1 9 1 8 2 NTNMOS W=15U L=15U AD=100P AS=100P
MC2 8 2 9 1 NTPMOS W=15U L=15U AD=100P AS=100P
*
*
*  Supply and measuring voltages
*
VDD  1  0  DC  5
VSS  0  2  DC  5
*
*  Compensating capacitor (use an appropriate
*  value like 3pF to start with)
*
CK  5  8  3PF
*
*  Include the desired load here
*
*
*  Perform dc analysis
*
.OP
*
*  Perform other analysis, and print/plot the results
*
*
*
.END
```

The results of this program are listed in table 3.4, along with the results assumed/derived in the design section

(section 3.2.1), for the sake of comparison. While other results of the simulation may be accepted, the results of drain current for M8 and M9 are not satisfactory. This could be because of increased VGS of M3 and M4 (2.417 volts, compared to the expected value of 2.25 volts).

3.2.2.2 AC analysis

Many changes were made to the W/L values listed in column 2 of table 3.4 before arriving at the final set of values. While some changes were made immediately after the first dc analysis run, other changes were made during the ac analysis to obtain reasonable ac small-signal gain, and to obtain the proper value of the series resistance in the compensation network. Since it involved a large number of runs of the SPICE program (dc and ac analysis), we will not describe exactly how we arrived at the final values. The final set of values are listed below:

Final W/L values

M1 and M2	:	56/26
M3 and M4	:	49/35
M6	:	9/64
M8	:	69/10
MC1 and MC2	:	15/13

Compensation capacitor value : 2.5 pF

***** The rest remain unchanged *****

Table 3.4 Results of hand calculation and first SPICE simulation run summarized for Op-amp # 2

DEVICE	W,L Microns	HAND CALCULATION			FIRST SIMULATION RUN		
		|VGS| Volts	|VTH| Volts	|ID| uA	|VGS| Volts	|VTH| Volts	|ID| uA
MB1	31,10	2.9	1.7	20	2.885	1.739	20.1
MB2	21,14	2.1	0.95	20	2.115	0.965	20.1
M1	51,25	1.65	0.95	10	1.709	0.978	10.2
M2	51,25	1.65	0.95	10	1.709	0.978	10.2
M3	50,38	2.25	0.95	10	2.417	0.991	10.2
M4	50,38	2.25	0.95	10	2.417	0.991	10.2
M5	21,14	2.1	0.95	20	2.115	0.962	20.5
M6	8,72	5.2	0.95	20	5.648	0.992	20.0
M7	21,14	2.1	0.95	20	2.115	0.966	20.0
M8	73,10	2.3	0.95	60	2.417	0.971	29.9
M9	25,10	2.5	0.95	60	1.935	0.926	29.9
DC VOLTAGE AT OUTPUT NODE FROM SIMULATION : 4.6937 Volts							

The necessary lines to be included for ac analysis in the SPICE program listed in section 3.2.2.1 are the following:

```
*
*   Include the load
*
RL  9   0   5MEG
CL  9   0   15PF
*
*   Include the ac signal, and
*     pulse input voltage
*
VIN  20   0   AC   0.0003
*VIN  21   0   PULSE(-1.0 1.0 1US 0S 0S 5US 10US)
*
*   Please see the special circuit
*     configuration required for
*     step-response (fig 3.5)
*
.TF   V(9)   VIN
.AC   DEC   8   1   10MEG
.PRINT   AC   VM(9)   VP(9)   VDB(9)
*    VDB(9) is the voltage of
*       node 9 in dB
*.TRAN   0.5US   30US
*.PLOT   TRAN   V(9)   V(21)
```

Notice that certain lines like *VIN 21 0 PULSE(.....) start with an asterisk. This means thay are insignificant as far as the program goes. This is one of the easier ways of switching between two types of analysis. The above-given lines of code are now set for a frequency response run, while the required commands for step-response have an asterisk at the beginning of each line (except comments). To set it for step-response run (described later), first remove the asterisk from the lines beginning with

```
*VIN.....
*.TRAN.....,and
*.PLOT
```

and then insert an asterisk in front of lines beginning with

```
VIN...........
.AC...........,and
.PRINT........
```

These results of frequency response run are listed below in a tabular form :

```
0****     SMALL-SIGNAL CHARACTERISTICS

0     V(9)/VIN                                  = -7.870E+03
0     INPUT RESISTANCE AT VIN                   =  1.000E+20
0     OUTPUT RESISTANCE AT V(9)                 =  3.062E+05

1***12-23-84 **** SPICE 2G.5A (23NOV82) ****23:54:41***

0OP-AMP # 2

0***  AC ANALYSIS       TEMPERATURE =   27.000 DEG C

0*************************************************************
```

X	FREQ	VM(9)	VP(9)	VDB(9)
	1.000E+00	2.361E+00	1.797E+02	7.461E+00
	1.259E+00	2.361E+00	1.797E+02	7.461E+00
	1.585E+00	2.361E+00	1.796E+02	7.461E+00
	1.995E+00	2.361E+00	1.795E+02	7.461E+00
	2.512E+00	2.361E+00	1.794E+02	7.461E+00
	3.162E+00	2.361E+00	1.792E+02	7.461E+00
	3.981E+00	2.361E+00	1.790E+02	7.460E+00
	5.012E+00	2.360E+00	1.787E+02	7.459E+00
	6.310E+00	2.360E+00	1.784E+02	7.458E+00
	7.943E+00	2.359E+00	1.780E+02	7.456E+00
	1.000E+01	2.359E+00	1.775E+02	7.453E+00
	1.259E+01	2.357E+00	1.768E+02	7.448E+00
	1.585E+01	2.355E+00	1.760E+02	7.440E+00
	1.995E+01	2.352E+00	1.749E+02	7.428E+00
	2.512E+01	2.346E+00	1.736E+02	7.408E+00
	3.162E+01	2.338E+00	1.720E+02	7.377E+00
	3.981E+01	2.325E+00	1.700E+02	7.328E+00

5.012E+01	2.305E+00	1.675E+02	7.252E+00
6.310E+01	2.273E+00	1.644E+02	7.134E+00
7.943E+01	2.227E+00	1.606E+02	6.953E+00
1.000E+02	2.158E+00	1.561E+02	6.681E+00
1.259E+02	2.061E+00	1.508E+02	6.282E+00
1.585E+02	1.931E+00	1.449E+02	5.716E+00
1.995E+02	1.768E+00	1.385E+02	4.947E+00
2.512E+02	1.576E+00	1.319E+02	3.954E+00
3.162E+02	1.370E+00	1.255E+02	2.734E+00
3.981E+02	1.163E+00	1.195E+02	1.311E+00
5.012E+02	9.681E-01	1.142E+02	-2.819E-01
6.310E+02	7.940E-01	1.096E+02	-2.004E+00
7.943E+02	6.443E-01	1.058E+02	-3.818E+00
1.000E+03	5.190E-01	1.027E+02	-5.697E+00
1.259E+03	4.159E-01	1.001E+02	-7.619E+00
1.585E+03	3.323E-01	9.802E+01	-9.569E+00
1.995E+03	2.649E-01	9.635E+01	-1.154E+01
2.512E+03	2.109E-01	9.501E+01	-1.352E+01
3.162E+03	1.678E-01	9.393E+01	-1.550E+01
3.981E+03	1.334E-01	9.306E+01	-1.750E+01
5.012E+03	1.060E-01	9.235E+01	-1.949E+01
6.310E+03	8.426E-02	9.176E+01	-2.149E+01
7.943E+03	6.694E-02	9.127E+01	-2.349E+01
1.000E+04	5.318E-02	9.085E+01	-2.548E+01
1.259E+04	4.225E-02	9.046E+01	-2.748E+01
1.585E+04	3.356E-02	9.011E+01	-2.948E+01
1.995E+04	2.666E-02	8.976E+01	-3.148E+01
2.512E+04	2.117E-02	8.940E+01	-3.348E+01
3.162E+04	1.682E-02	8.900E+01	-3.548E+01
3.981E+04	1.336E-02	8.855E+01	-3.749E+01
5.012E+04	1.061E-02	8.803E+01	-3.949E+01
6.310E+04	8.423E-03	8.740E+01	-4.149E+01
7.943E+04	6.688E-03	8.663E+01	-4.349E+01
1.000E+05	5.308E-03	8.568E+01	-4.550E+01
1.259E+05	4.211E-03	8.451E+01	-4.751E+01
1.585E+05	3.338E-03	8.304E+01	-4.953E+01
1.995E+05	2.643E-03	8.122E+01	-5.156E+01
2.512E+05	2.088E-03	7.894E+01	-5.360E+01
3.162E+05	1.646E-03	7.610E+01	-5.567E+01
3.981E+05	1.291E-03	7.259E+01	-5.778E+01
5.012E+05	1.005E-03	6.826E+01	-5.995E+01
6.310E+05	7.750E-04	6.300E+01	-6.221E+01
7.943E+05	5.883E-04	5.672E+01	-6.461E+01
1.000E+06	4.370E-04	4.941E+01	-6.719E+01
1.259E+06	3.154E-04	4.121E+01	-7.002E+01
1.585E+06	2.197E-04	3.247E+01	-7.316E+01
1.995E+06	1.471E-04	2.372E+01	-7.665E+01
2.512E+06	9.470E-05	1.562E+01	-8.047E+01
3.162E+06	5.897E-05	8.794E+00	-8.459E+01
3.981E+06	3.589E-05	3.649E+00	-8.890E+01
5.012E+06	2.161E-05	2.746E-01	-9.331E+01
6.310E+06	1.302E-05	-1.533E+00	-9.771E+01
7.943E+06	7.899E-06	-2.146E+00	-1.020E+02
1.000E+07	4.846E-06	-1.961E+00	-1.063E+02

```
  1.259E+07     3.009E-06  -1.313E+00  -1.104E+02
  1.585E+07     1.893E-06  -4.649E-01  -1.145E+02
  1.995E+07     1.207E-06   3.396E-01  -1.184E+02
  2.512E+07     7.812E-07   8.206E-01  -1.221E+02
  3.162E+07     5.128E-07   6.367E-01  -1.258E+02
  3.981E+07     3.407E-07  -5.581E-01  -1.294E+02
  5.012E+07     2.282E-07  -2.995E+00  -1.328E+02
Y
0
        JOB CONCLUDED
```

Observe that the unity gain frequency is about 1.259 MHz, and at this point we have a phase margin of about 40 degrees.

Step Response

Step response is one of the important tests that can be conducted on an Op-amp to ascertain its performance. From the step response we can determine the rise time, fall time, settling time etc. A proper output for a step-response test indicates that the Op-amp is stable.

Figure 3.5 shows the usual configuration adopted for step response study. There is 100% negative feedback and a pulse is applied to the positive input terminal (if needed, through a resistor R_s). The output is viewed on an oscilloscope. At the output the type of response that can be expected is also shown in the figure. Observe the ringing in the output waveform. It should be small.

This circuit can easily be simulated on SPICE using PULSE and .TRAN commands. The required commands are given below:

```
VIN 21 0 PULSE(-1 1 0S 0S 0S 5US 10US)
*
```

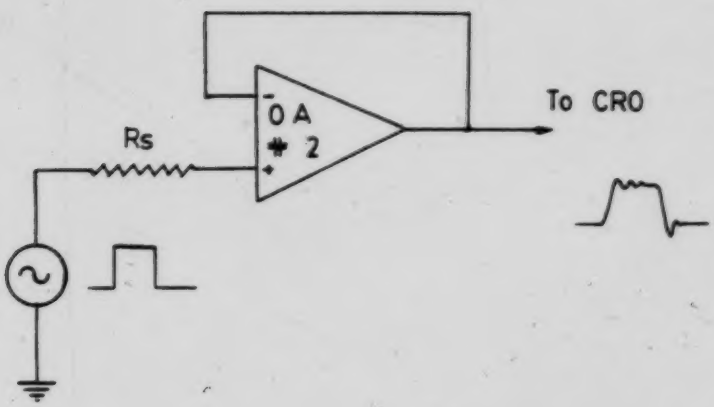


Figure 3.5 Circuit configuration for step response study of an Op-amp

```
*   This gives a pulse of 2 volt amplitude
*     and 10 microsecond period with 50%
*     duty cycle.  The gate of M1 should
*     connected to the output node.
*
.TRAN  0.5S  30US
.PLOT  TRAN  V(9)  V(21)
*
```

The resulting waveform at the output node is shown in the following page. Observe a finite rise and fall time, and small ringing.

3.2.3 Layout Preparation

After finalizing all the W/L values and the compensation capacitor value, some time was spent on planning the layout. By modifying the structure of the input transistors, it is possible to make the Op-amp circuit work as a magnetic field sensor. (See chapter 4 for further details). To incorporate this, some space was left free around the input transistors M1 and M2. The area required for the compensation capacitor of 2.5 pF was calculated as follows :

From reference [7], poly-to-poly capacitance

$= 3.1 \pm 0.2E\text{-}08$ F/cm²

The plus or minus value was neglected.

3.1E-08 F → 1 cm²

So for 1 pF → [(1E-12 x 1)/3.1 E-08] cm²

= 0.3225807E-04 cm²

= 0.3225807 x 1E-04 x 1E-04 m²

= 0.3225807 x 1E-08 x 1E+12 sq.microns

```
1********12-24-84 ********  SPICE 2B.5A (23NOV82) *********00:21:32******

OOP-AMP # 2

0*****     TRANSIENT ANALYSIS                TEMPERATURE =   27.000 DEG C

0*************************************************************************


OLEGEND:

 *: V(9)
 +: V(21)
X
     TIME       V(9)

X(*+)------------ -2.000E+00     -1.000E+00      0.0           1.000E+00  2.000E+00
                  - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  0.0          -9.999E-01 .            X             .             .          .
  5.000E-07    -1.000E+00 .            X             .             .          .
  1.000E-06    -1.000E+00 .            X             .             .          .
  1.500E-06     5.963E-01 .            .             .          *  +          .
  2.000E-06     9.786E-01 .            .             .             X          .
  2.500E-06     1.030E+00 .            .             .             X          .
  3.000E-06     9.897E-01 .            .             .             X          .
  3.500E-06     1.009E+00 .            .             .             X          .
  4.000E-06     9.984E-01 .            .             .             X          .
  4.500E-06     9.966E-01 .            .             .             X          .
  5.000E-06     1.002E+00 .            .             .             X          .
  5.500E-06     1.001E+00 .            .             .             X          .
  6.000E-06     9.949E-01 .            .             .             X          .
  6.500E-06     1.005E+00 .            .             .             X          .
  7.000E-06    -5.824E-01 .            +     *       .             .          .
  7.500E-06    -9.767E-01 .            X             .             .          .
  8.000E-06    -1.030E+00 .            X             .             .          .
  8.500E-06    -9.824E-01 .            X             .             .          .
  9.000E-06    -1.012E+00 .            X             .             .          .
  9.500E-06    -9.974E-01 .            X             .             .          .
  1.000E-05    -9.949E-01 .            X             .             .          .
  1.050E-05    -1.004E+00 .            X             .             .          .
  1.100E-05    -9.951E-01 .            X             .             .          .
  1.150E-05     6.118E-01 .            .             .          *  +          .
  1.200E-05     9.832E-01 .            .             .             X          .
  1.250E-05     1.037E+00 .            .             .             +*         .
  1.300E-05     9.921E-01 .            .             .             X          .
  1.350E-05     1.006E+00 .            .             .             X          .
  1.400E-05     1.001E+00 .            .             .             X          .
  1.450E-05     9.953E-01 .            .             .             X          .
  1.500E-05     1.001E+00 .            .             .             X          .
  1.550E-05     1.004E+00 .            .             .             X          .
  1.600E-05     9.934E-01 .            .             .             X          .
  1.650E-05     1.005E+00 .            .             .             X          .
  1.700E-05    -5.827E-01 .            +     *       .             .          .
  1.750E-05    -9.688E-01 .            X             .             .          .
  1.800E-05    -1.031E+00 .            X             .             .          .
  1.850E-05    -9.841E-01 .            X             .             .          .
  1.900E-05    -1.015E+00 .            X             .             .          .
  1.950E-05    -9.968E-01 .            X             .             .          .
  2.000E-05    -9.954E-01 .            X             .             .          .
  2.050E-05    -1.003E+00 .            X             .             .          .
  2.100E-05    -9.946E-01 .            X             .             .          .
  2.150E-05     6.019E-01 .            .             .          *  +          .
  2.200E-05     9.852E-01 .            .             .             X          .
                  - - - - - - - - - - - - - - - - - - - - - - - - - - - - -


Y
0

        JOB CONCLUDED
0        TOTAL JOB TIME            0.0
```

Area for 1 pF = 3225.807 sq.microns .....(4.3)

So for 2.5 pF we need an area of 2.5 x (3225.807) = 8064.5 sq.microns. For this a convenient value of 50 μ x 161 μ (= 8050 sq.microns) was taken.

As in the case of Op-amp # 1, the complete layout was first drawn using a big graph-sheet, making sure that the design rules are not violated. This was then coded using the AHF language. The AMDHAL computer of University of Alberta was used to convert the AHF code to CIF code, for transportation to the fabrication house. A CALCOMP plot of the layout and the AHF code listing are given in Appendix A.

3.2.4 Final Simulation Results

From the layout drawn on a big graph-sheet, the exact values of drain and source area, drain and source perimeter, and number of squares on drain and source were measured for each transistor. This was substituted in place of assumed/default values in the SPICE program and the simulation was carried out one more time. The results of this (final) simulation run are given in table 3.5

3.2.5 Design Observations

1. In the case of transistors M3 and M4, a relatively higher value of L would increase the drain-to-source resistance. This increase in resistance will aid in increasing the gain of the differential stage.
2. The size of the transistors MC1 and MC2 becomes crucial

Table 3.5 Final simulation results for Op-amp # 2

DEVICE	|ID| uA	|VGS| Volts	|VDS| Volts	|VTH| Volts
M1	10.2	1.692	4.322	0.979
M2	10.2	1.692	4.322	0.979
M3	10.2	2.37	2.37	0.99
M4	10.2	2.37	2.37	0.99
M5	20.5	2.116	3.308	0.961
M6	20.2	5.134	7.504	0.991
M7	20.2	2.116	2.496	0.964
M8	67.4	2.37	4.817	0.954
M9	67.3	2.496	5.183	0.937
MB1	20.1	2.884	2.884	1.793
MB2	20.1	2.116	2.116	0.965

DC Open-Loop Gain	: 7818(77.9dB)
Unity Gain Frequency	: 1.26 MHz
Phase Margin	: 40 degrees
Supply Current IDD	: 108 uA
Supply Current ISS	: 128 uA
Power Dissipation	: 1.18 mW
Slew Rate	: 1.65 v/µSec
Die Area	: 0.464 sq.mm (720 sq.mils)

in the step response test using SPICE. A large number of trials with different values for MC1 and MC2 may be required to get a step response that converges and gives proper results.

3. Because we have a p-well process, any number of n-type transistors can be realized with their base-to-source voltage VBS equal to zero just by separate p-wells for each transistor. By doing so we can eliminate the variation in threshold voltage. This is not possible with p-type transistors.

3.3 OP - AMP # 3

This section deals with the design and analysis of an Op-amp that has p-type input transistors, and a cascode differential stage. As this is the third Op-amp discussed in this thesis, it is henceforth called Op-amp # 3. Since the design and analysis methodology is the same as given in the previous sections, more emphasis is placed on the presentation of results, and less on verbal description.

3.3.1 Design of the circuit

Figure 3.6 shows the circuit diagram of Op-amp # 3. VDD is taken as +5 volts, and VSS as -5 volts. As in the previous chapter, all transistors, except MC1 and MC2 are assumed to operate in the pinch-off region, so that equation (3.2) can be used to calculate the aspect ratio (W/L). Since the design procedure is almost identical to that of Op-amp #

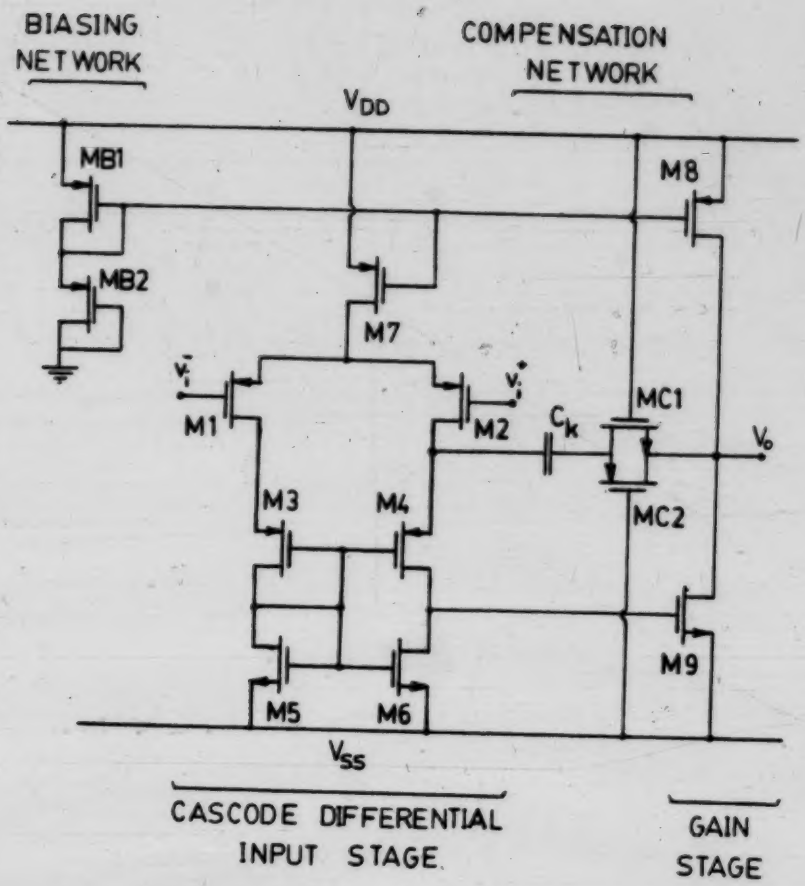


Figure 3.6 Circuit diagram of Op-amp # 3

2, in this section we present only the final design parameters in a tabular manner. In table 3.6, which summarizes the design procedure, values inside the bracket are assumed values. Those values that have a star (*) superscript are logically deduced values. Others are calculated values. Here all threshold voltages are put under 'Logically deduced' category since they are either the value specified by Northern Telecom process, or are read from a graph of VBS versus VTH, supplied by Northern Telecom [7].

3.3.2 SPICE Simulation

As before, a program can be written in SPICE to determine the accurate operating points, and the ac parameters. Figure 5.2 shows the node assignments for SPICE program and the W/L values used for the first dc analysis run of the SPICE program.

3.3.2.1 DC analysis

Refering to figure 3.7, a SPICE program can be written, in a manner similar to that described in the previous two chapters. The program is listed below, and the results of this program are given in table 3.7, along with the hand-calculated values.

```
OP-AMP # 3
*
*   Select appropriate options from
*     .OPTIONS card
*
.OPTIONS NOMOD ABSTOL=1N VNTOL=1U CPTIME=10 NUMDGT=4
```

Table 3.6 Summary of design procedure for Op-amp # 3

DEV.	TYPE	|ID| uA	|VGS| Volts	|VTH| Volts	W L from eq.4.1	SELECT	
						W	L
MB1	p	(15)	(2.25)	0.95*	1.972	30	15
MB2	p	(15)	2.75*	1.45*	1.972	20	10
M1	p	(22.5)	(2.5)	1.5*	5	50	10
M2	p	(22.5)	(2.5)	1.5*	5	50	10
M3	p	(22.5)	(2.5)	1.8*	10.2	100	10
M4	p	(22.5)	(2.5)	1.8*	10.2	100	10
M5	n	(22.5)	(2.0)	.95*	2.04	100	50
M6	n	(22.5)	(2.0)	.95*	2.04	100	50
M7	p	(45)	2.25*	.95*	5.92	90*	15*
M8	p	(70)	2.25*	.95*	9.204	92	10
M9	n	(70)	2.2*	.95*	4.48	45	10

(Inside bracket) : Assumed value
With a star* : Logically deduced value
Otherwise : Calculated value

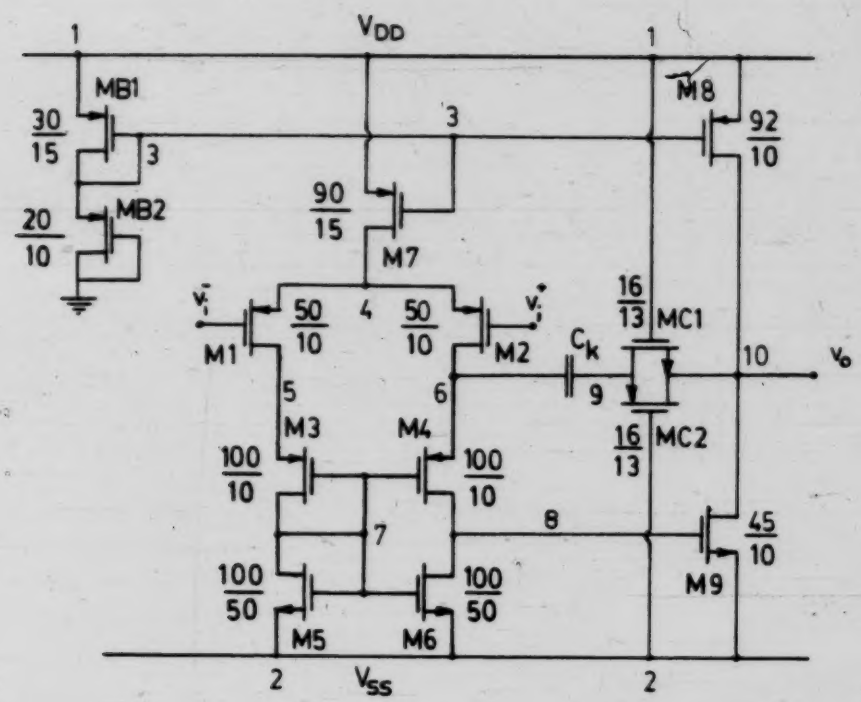


Figure 3.7 Op-amp # 3 : node assignment for SPICE program, and W/L values for first dc analysis program in SPICE

```
*
.WIDTH IN=80 OUT=70
*
*   Use .MODEL card to describe the NT CMOS-1B
*     process.  First NMOS, then PMOS
*
.MODEL NTNMOS NMOS(LEVEL=2 VTO=1.0 PB=0.7
+ CGSO=4.0E-10  CGDO=4.0E-10  CGBO=2.0E-10  RSH=15.0
+ CJ=4.0E-4     MJ=2.0        CJSW=8.0E-10  MJSW=2.0
+ JS=1.0E-6     TOX=8.5E-8    NSUB=1.0E16   XJ=1.0E-6
+ LD=0.7E-6     UO=750        UCRIT=5.0E4   UEXP=0.14
+ VMAX=5.0E4)
*
*
*
.MODEL NTPMOS PMOS(LEVEL=2 VTO=-1.0 PB=0.7
+ CGSO=4.0E-10  CGDO=4.0E-10  CGBO=2.0E-10  RSH=75.0
+ CJ=1.8E-4     MJ=2.0        CJSW=6.0E-10  MJSW=2.0
+ JS=1.0E-6     TOX=8.5E-8    NSUB=2.0E15   XJ=0.9E-6
+ LD=0.6E-6     UO=250        UCRIT=1.0E4   UEXP=0.03
+ VMAX=3.0E4)
*
*  Circuit description, refer to figure 3.7
*
*
MB1   3  3  1  1  NTPMOS  W=30U   L=15U   AD=100P  AS=100P
MB2   0  0  3  1  NTPMOS  W=19.5U L=10U   AD=100P  AS=100P
M1    5 10  4  1  NTPMOS  W=52U   L=12U   AD=250P  AS=250P
M2    6 21  4  1  NTPMOS  W=52U   L=12U   AD=250P  AS=250P
M3    7  7  5  1  NTPMOS  W=100U  L=10U   AD=300P  AS=300P
M4    8  7  6  1  NTPMOS  W=100U  L=10U   AD=300P  AS=300P
M5    7  7  2  2  NTNMOS  W=100U  L=50U   AD=400P  AS=400P
M6    8  7  2  2  NTNMOS  W=100U  L=50U   AD=400P  AS=400P
M7    4  3  1  1  NTPMOS  W=90U   L=15U   AD=300P  AS=300P
M8   10  8  2  2  NTNMOS  W=47U   L=10U   AD=250P  AS=250P
M9   10  3  1  1  NTPMOS  W=80U   L=10U   AD=450P  AS=450P
MC1   9  1 10  2  NTNMOS  W=16U   L=13U   AD=100P  AS=100P
MC2  10  2  9  1  NTPMOS  W=16U   L=13U   AD=100P  AS=100P
*
*
CK1   9  6  4.0PF
*
*
*  Voltages
*
VDD   1  0  DC  5
VSS   0  2  DC  5
*
*   Perform the dc analysis
*
.OP
*
*
.END
```

3.3.2.2 AC Analysis

A number of small changes were made to the W and L values given in the last two columns of table 3.6 Some of them were made to bring the dc voltage of the output node close to zero. Others were required to improve some ac small-signal parameters. A number of trials of the step-response were required to finalize the values of MC1 and MC2. The final W and L values for the transistors of figure 3.6 are given in table 3.8

For ac analysis the following lines of code are required in addition to the program listed in section 3.3.2.1. Also the final Width and Length values, listed in table 3.8, are used.

```
*
*   Include the load
*
RL   10   0   5MEG
CL   10   0   15PF
*
*   For ac small-signal analysis
*     inclued the following lines
VIN   20   0   AC  0.0001
.TF   V(10)   VIN
.AC   DEC   8   1   10MEG
.PRINT   AC   VM(10)   VDB(10)   VP(10)
*
*   For step-response include the
*     following lines  (See figure
*     3.5 for step response circuit
*     configuration)
VIN 21 0 PULSE(-0.5 0.5 1US 0S 0S 5US 10US)
.TRAN   0.5US   30US
.PLOT   TRAN   V(10)   V(21)
```

Table 3.7 Hand-calculated values compared with the results of first SPICE simulation run for Op-amp # 3

DEVICE	W,L Microns	HAND CALCULATION			FIRST SIMULATION RUN		
		|VGS| Volts	|VTH| Volts	|ID| uA	|VGS| Volts	|VTH| Volts	|ID| uA
MB1	30,15	2.25	0.95	15	2.325	0.975	15.2
MB2	20,15	2.75	1.45	15	2.675	1.463	15.2
M1	50,10	2.50	1.50	22.5	2.427	1.499	22.8
M2	50,10	2.50	1.50	22.5	2.427	1.499	22.8
M3	100,10	2.50	1.80	22.5	2.479	1.836	22.8
M4	100,10	2.50	1.80	22.5	2.479	1.836	22.8
M5	100,10	2.0	0.95	22.5	2.114	0.991	22.8
M6	100,50	2.0	0.95	22.5	2.114	0.991	22.8
M7	90,15	2.25	0.95	45	2.325	0.975	45.6
M8	92,10	2.25	0.95	70	2.325	0.965	73.7
M9	45,10	2.2	0.95	70	2.114	0.929	73.7
DC VOLTAGE AT OUTPUT NODE FROM SIMULATION : 3.3696 Volts							

Table 3.8 Final Length and Width values for the transistors of figure 3.6 (Op-amp # 3)

DEVICE	WIDTH Microns	LENGTH Microns
MB1	30	15
MB2	19.5	10
M1	52	12
M2	52	12
M3	100	10
M4	100	10
M5	100	50
M6	100	50
M7	90	15
M8	80	10
M9	47	10
MC1	16	13
MC2	16	13
COMPENSATION CAPACITOR : 4pF		

The results of the above two runs are given below:

Results of frequency response run

```
0****     SMALL-SIGNAL CHARACTERISTICS

0     V(10)/VIN                          = -1.214E+04
0     INPUT RESISTANCE AT VIN            =  1.000E+20
0     OUTPUT RESISTANCE AT V(10)         =  2.795E+05


1***01-08-85 ***  SPICE 2G.5A (23NOV82) ***15:17:18***

0 OP - AMP # 3
0***     AC ANALYSIS    TEMPERATURE =   27.000 DEG C

0**************************************************************

     FREQ         VM(10)       VDB(10)      VP(10)
X

  1.000E+00     1.214E+00    1.685E+00    1.796E+02
  1.259E+00     1.214E+00    1.684E+00    1.795E+02
  1.585E+00     1.214E+00    1.684E+00    1.794E+02
  1.995E+00     1.214E+00    1.684E+00    1.792E+02
  2.512E+00     1.214E+00    1.683E+00    1.790E+02
  3.162E+00     1.214E+00    1.683E+00    1.787E+02
  3.981E+00     1.214E+00    1.681E+00    1.784E+02
  5.012E+00     1.213E+00    1.679E+00    1.779E+02
  6.310E+00     1.213E+00    1.676E+00    1.774E+02
  7.943E+00     1.212E+00    1.671E+00    1.767E+02
  1.000E+01     1.211E+00    1.663E+00    1.759E+02
  1.259E+01     1.209E+00    1.650E+00    1.749E+02
  1.585E+01     1.206E+00    1.629E+00    1.735E+02
  1.995E+01     1.202E+00    1.597E+00    1.719E+02
  2.512E+01     1.195E+00    1.547E+00    1.698E+02
  3.162E+01     1.184E+00    1.468E+00    1.672E+02
  3.981E+01     1.168E+00    1.346E+00    1.641E+02
  5.012E+01     1.143E+00    1.159E+00    1.603E+02
  6.310E+01     1.106E+00    8.788E-01    1.557E+02
  7.943E+01     1.055E+00    4.685E-01    1.504E+02
  1.000E+02     9.873E-01   -1.114E-01    1.444E+02
  1.259E+02     9.019E-01   -8.964E-01    1.380E+02
  1.585E+02     8.028E-01   -1.907E+00    1.314E+02
  1.995E+02     6.964E-01   -3.143E+00    1.250E+02
  2.512E+02     5.901E-01   -4.581E+00    1.191E+02
  3.162E+02     4.907E-01   -6.185E+00    1.138E+02
  3.981E+02     4.020E-01   -7.915E+00    1.093E+02
  5.012E+02     3.260E-01   -9.735E+00    1.056E+02
  6.310E+02     2.625E-01   -1.162E+01    1.025E+02
  7.943E+02     2.103E-01   -1.354E+01    9.999E+01
  1.000E+03     1.680E-01   -1.549E+01    9.797E+01
```

1.259E+03	1.339E-01	-1.746E+01	9.635E+01
1.585E+03	1.066E-01	-1.944E+01	9.506E+01
1.995E+03	8.481E-02	-2.143E+01	9.404E+01
2.512E+03	6.743E-02	-2.342E+01	9.323E+01
3.162E+03	5.359E-02	-2.542E+01	9.258E+01
3.981E+03	4.258E-02	-2.742E+01	9.208E+01
5.012E+03	3.383E-02	-2.941E+01	9.168E+01
6.310E+03	2.688E-02	-3.141E+01	9.137E+01
7.943E+03	2.135E-02	-3.341E+01	9.114E+01
1.000E+04	1.696E-02	-3.541E+01	9.097E+01
1.259E+04	1.347E-02	-3.741E+01	9.085E+01
1.585E+04	1.070E-02	-3.941E+01	9.077E+01
1.995E+04	8.502E-03	-4.141E+01	9.073E+01
2.512E+04	6.754E-03	-4.341E+01	9.074E+01
3.162E+04	5.365E-03	-4.541E+01	9.078E+01
3.981E+04	4.263E-03	-4.741E+01	9.086E+01
5.012E+04	3.387E-03	-4.940E+01	9.099E+01
6.310E+04	2.691E-03	-5.140E+01	9.118E+01
7.943E+04	2.139E-03	-5.340E+01	9.142E+01
1.000E+05	1.701E-03	-5.539E+01	9.174E+01
1.259E+05	1.353E-03	-5.737E+01	9.214E+01
1.585E+05	1.077E-03	-5.935E+01	9.265E+01
1.995E+05	8.589E-04	-6.132E+01	9.329E+01
2.512E+05	6.863E-04	-6.327E+01	9.407E+01
3.162E+05	5.501E-04	-6.519E+01	9.500E+01
3.981E+05	4.430E-04	-6.707E+01	9.609E+01
5.012E+05	3.592E-04	-6.889E+01	9.728E+01
6.310E+05	2.939E-04	-7.064E+01	9.850E+01
7.943E+05	2.433E-04	-7.228E+01	9.955E+01
1.000E+06	2.041E-04	-7.380E+01	1.002E+02
1.259E+06	1.736E-04	-7.521E+01	1.001E+02
1.585E+06	1.496E-04	-7.650E+01	9.891E+01
1.995E+06	1.304E-04	-7.769E+01	9.640E+01
2.512E+06	1.156E-04	-7.874E+01	9.225E+01
3.162E+06	1.050E-04	-7.957E+01	8.572E+01
3.981E+06	9.956E-05	-8.004E+01	7.473E+01
5.012E+06	9.751E-05	-8.022E+01	5.342E+01
6.310E+06	7.852E-05	-8.210E+01	1.435E+01
7.943E+06	3.939E-05	-8.809E+01	-2.135E+01
1.000E+07	1.759E-05	-9.509E+01	-3.875E+01
1.259E+07	8.363E-06	-1.016E+02	-4.671E+01
1.585E+07	4.266E-06	-1.074E+02	-5.069E+01
1.995E+07	2.317E-06	-1.127E+02	-5.323E+01
2.512E+07	1.331E-06	-1.175E+02	-5.597E+01
3.162E+07	8.028E-07	-1.219E+02	-6.020E+01
3.981E+07	5.018E-07	-1.260E+02	-6.679E+01

Y
0

JOB CONCLUDED
0 TOTAL JOB TIME 0.0

Results of step response run

The computer print-out of the step-response run is given in the next page.

3.3.3 Layout

As in the case of Op-amp # 2, some space was left around the input transistors M1 and M2 for modification later on (see the CALCOMP plot attached in Appendix A). Compensation capacitance value was determined using equation (3.4) Area for 4pF = 4 (Area for 1 pF)

= 4(3225.807)

= 12903 sq.microns

A convenient value of 234.5 microns x 55 microns (= 12897.5 sq.microns) was chosen for the compensation capacitor.

The complete layout was prepared carefully on a big graph-sheet and coded in AHF language. The AHF code listing and a CALCOMP plot of the layout may be found in Appendix A.

3.3.4 Final Simulation Results

From original (hand-drawn) layout the various values of drain and source area, drain and source perimeters, and number of squares on drain and source are measured for each transistor, and substituted back into the SPICE program. The program is run once more, this time using the exact values instead of assumed/default values. The results of this simulation is taken as the final value. The results are

```
1********01-31-85 ********  SPICE 2G.5A (23NOV82) ********17:18:08******

OOP - AMP # 3

0*****     TRANSIENT ANALYSIS                TEMPERATURE =   27.000 DEG C

0*****************************************************************************

OLEGEND:

 *: V(10)
 +: V(21)
X
     TIME       V(10)

X(*+)------------ -1.000E+00    -5.000E-01     0.0          5.000E-01  1.000E+00
                  ---------------------------------------------------------
  0.0        -5.000E-01 .            X          .            .          .
 5.000E-07   -5.000E-01 .            X          .            .          .
 1.000E-06   -5.000E-01 .            X          .            .          .
 1.500E-06    3.100E-01 .            .          .         *  +          .
 2.000E-06    4.732E-01 .            .          .            *+         .
 2.500E-06    5.018E-01 .            .          .            X          .
 3.000E-06    5.120E-01 .            .          .            X          .
 3.500E-06    5.007E-01 .            .          .            X          .
 4.000E-06    4.912E-01 .            .          .            X          .
 4.500E-06    5.032E-01 .            .          .            X          .
 5.000E-06    4.979E-01 .            .          .            X          .
 5.500E-06    5.030E-01 .            .          .            X          .
 6.000E-06    4.940E-01 .            .          .            X          .
 6.500E-06    5.137E-01 .            .          .            X          .
 7.000E-06   -3.169E-01 .            +    *     .            .          .
 7.500E-06   -4.839E-01 .            X          .            .          .
 8.000E-06   -4.969E-01 .            X          .            .          .
 8.500E-06   -5.024E-01 .            X          .            .          .
 9.000E-06   -5.028E-01 .            X          .            .          .
 9.500E-06   -4.947E-01 .            X          .            .          .
 1.000E-05   -5.074E-01 .            X          .            .          .
 1.050E-05   -4.927E-01 .            X          .            .          .
 1.100E-05   -5.031E-01 .            X          .            .          .
 1.150E-05    3.205E-01 .            .          .         *  +          .
 1.200E-05    4.756E-01 .            .          .            *+         .
 1.250E-05    4.971E-01 .            .          .            X          .
 1.300E-05    4.936E-01 .            .          .            X          .
 1.350E-05    4.831E-01 .            .          .            X          .
 1.400E-05    5.043E-01 .            .          .            X          .
 1.450E-05    5.003E-01 .            .          .            X          .
 1.500E-05    4.982E-01 .            .          .            X          .
 1.550E-05    5.008E-01 .            .          .            X          .
 1.600E-05    5.021E-01 .            .          .            X          .
 1.650E-05    5.167E-01 .            .          .            X          .
 1.700E-05   -3.181E-01 .            +    *     .            .          .
 1.750E-05   -4.914E-01 .            X          .            .          .
 1.800E-05   -4.927E-01 .            X          .            .          .
 1.850E-05   -4.985E-01 .            X          .            .          .
 1.900E-05   -5.014E-01 .            X          .            .          .
 1.950E-05   -5.003E-01 .            X          .            .          .
 2.000E-05   -4.992E-01 .            X          .            .          .
 2.050E-05   -5.002E-01 .            X          .            .          .
 2.100E-05   -5.082E-01 .            X          .            .          .
 2.150E-05    3.219E-01 .            .          .         *  +          .
 2.200E-05    4.777E-01 .            .          .            *+         .
                  ---------------------------------------------------------
Y
0

        JOB CONCLUDED
0        TOTAL JOB TIME            0.0
```

given in table 3.9

3.3.5 Design Observations

1. In order to push the zero given by equation 2.26 to infinity, transistors MC1 and MC2 in parallel should present a resistance R_z that is equal to the reciprocal of the transconductance of the second stage. This may be little hard to realize. Fortunately there is a way out. If R_z is made greater than $1/g_{m2}$, the zero will move to the left-half plane, and this has been found to improve the phase margin[12]. So we can make R_z to be slightly greater than $1/g_{m2}$.
2. A higher value of the drain-to-source resistance of transistor M7 would increase the CMRR (see equation 2.25)

Table 3.9 Final simulation results for Op-amp # 3

DEVICE	|ID| uA	|VGS| Volts	|VDS| Volts	|VTH| Volts
M1	22.6	2.525	2.941	1.509
M2	22.6	2.525	2.941	1.509
M3	22.6	2.476	2.476	1.837
M4	22.6	2.476	2.476	1.837
M5	22.6	2.109	2.109	0.991
M6	22.6	2.109	2.109	0.991
M7	45.3	2.317	2.475	0.975
M8	72.8	2.317	4.931	0.954
M9	72.8	2.109	5.069	0.937
MB1	15.0	2.317	2.317	0.975
MB2	15.0	2.683	2.683	1.462

DC Open-Loop Gain	: 12070(81.6dB)
Unity Gain Frequency	: 3.20 MHz
Phase Margin	: 75 degrees
Supply Current IDD	: 133 uA
Supply Current ISS	: 118 uA
Power Dissipation	: 1.26 mW
Slew Rate	: 1.65 v/µSec
Die Area	: 0.51 sq.mm (790 sq.mils)

4. CMOS OP-AMP AS MAGNETIC FIELD SENSOR

This chapter considers the possibility of using a CMOS Op-amp as a magnetic field sensor by making small changes to the structure of the two input transistors. No formal mathematical treatment is given, but only a verbal description.

4.1 Principle of Operation

Consider the differential stage of Op-amp # 3 (see figure 3.6), whose transistors M1 and M2 are shown seperately in figure 4.1 (a). A typical way of realizing these transistors in a standard CMOS process is shown in figure 4.1 (b). The current ID1 and ID2 through each of the two transistors M1 and M2 can be varied by applying a differential potential to the two gates. (See section 2.5, MOS differential pair).

Now consider the modified structure, shown in figure 4.2, for the realization of M1 and M2 of figure 4.1 (a). This has a common source at the top of a fairly large rectangular area of diffusion called the 'Drifting Area'. The two transistors M1 and M2 are realized at the bottom, as shown. Now if the gate potentials are the same and assuming defect-free fabrication, then because of the perfect symmetry, we can say that both the drain currents will be equal. However the drain currents can be changed, as in the previous case, by applying a differential potential to the gates.

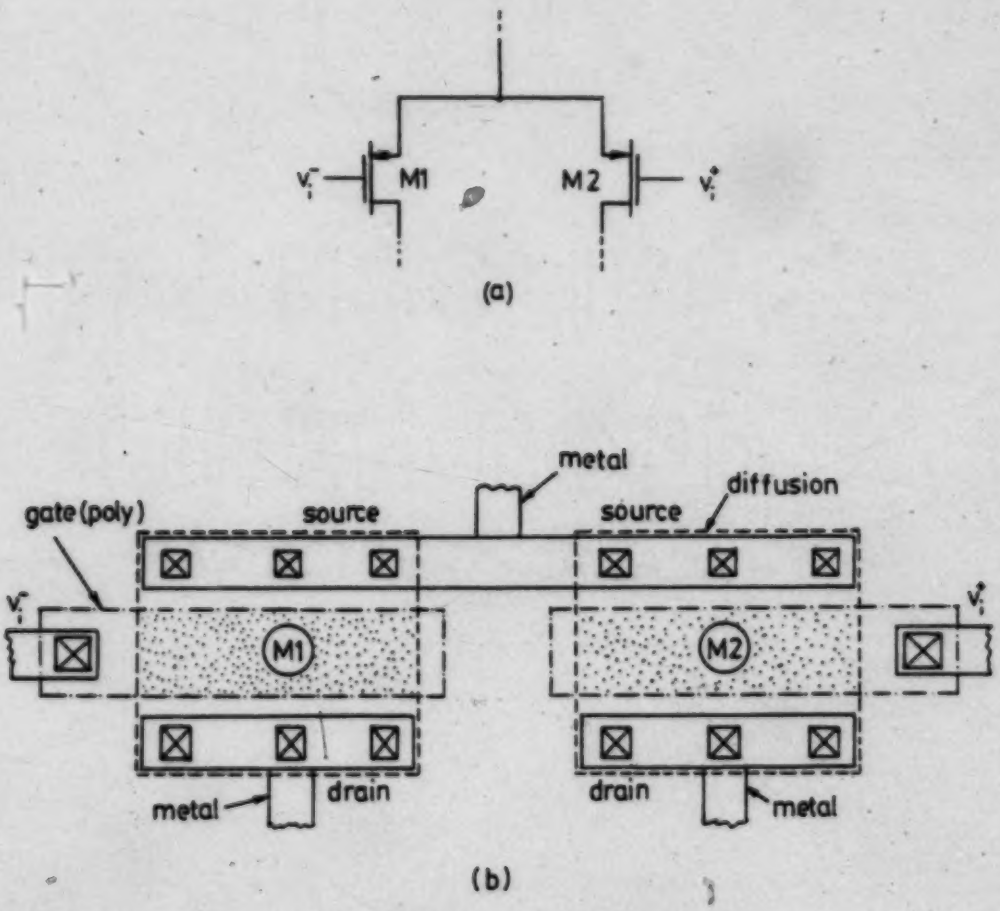


Figure 4.1 (a) Circuit diagram showing the input transistors in a differential stage; (b) Typical realization of the above circuit in a standard CMOS process

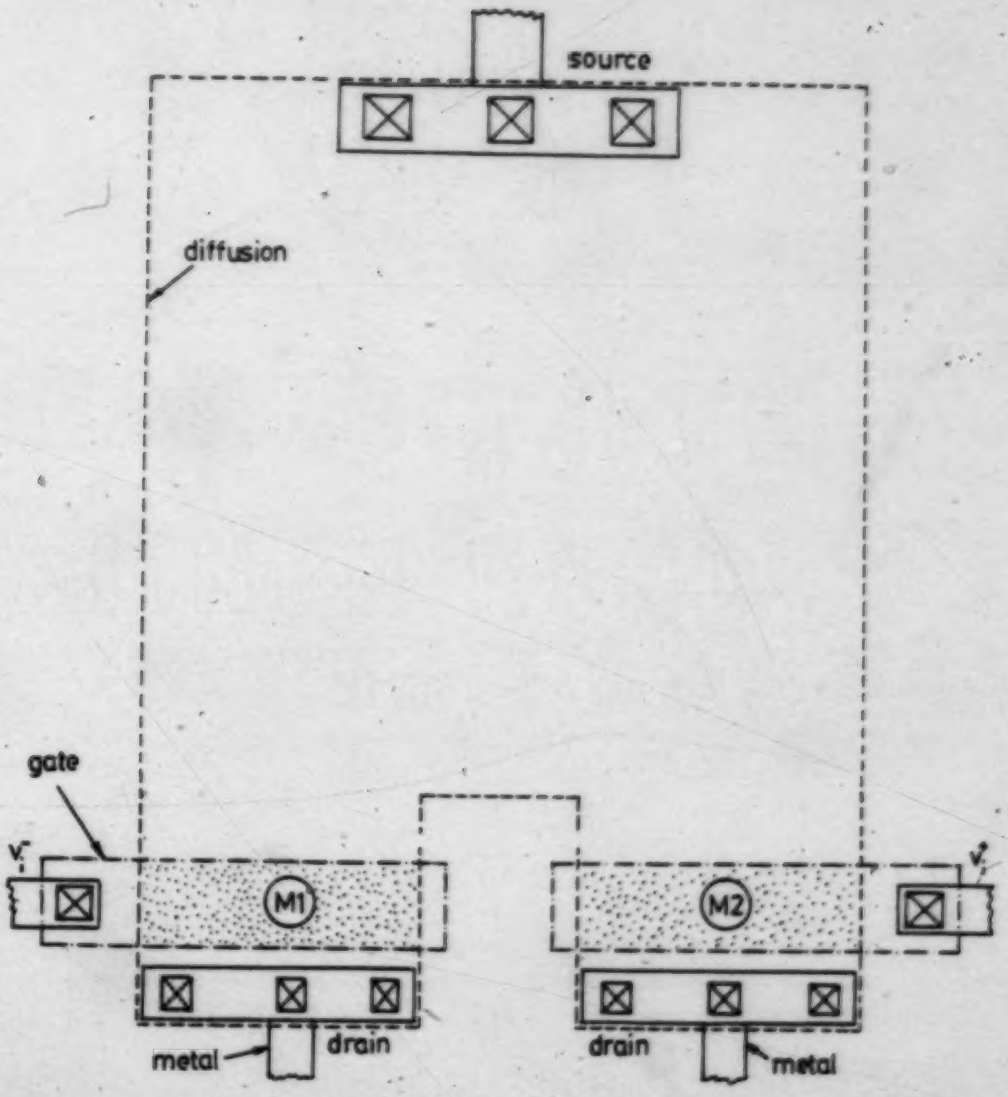


Figure 4.2 New structure of input transistors for making Op-amps sensitive to magnetic field

Assume that the two gate potentials are exactly equal, and that a steady magnetic field is applied into the plane of the paper. We now have a stream of holes (majority carriers in the p+ implanted source region) flowing from the common source to the two transistors, and a steady magnetic field into the plane of the paper. From Lorentz's equation, we can expect a carrier deflection. This will result in electron crowding at one end (transistor M1) and a scarcity of electrons at the other end (transistor M2). In that case we can expect the current through one of the transistors to be larger than the current through the other. This may be viewed as equivalent to the application of a differential potential to the gates, and therefore the dc output voltage deviates from its initial value of zero. Thus we can expect to have an output voltage because of the presence of magnetic field.

4.2 Layout Modifications and Expected Results

The input section of Op-amp # 2 and Op-amp # 3 were modified to include the structure shown in figure 4.2. The modified version has been sent for fabrication, but the fabricated version has not yet been received.

As discussed in section 4.1, we can expect the device to be sensitive to magnetic fields. How sensitive is it? Will it be linear? If so up to what range? When does the saturation begin? How does these properties depend on the device geometry and the 'Drifting Area'? These are some of

the interesting questions to be answered, once we know that the circuit works as expected. Therefore we decided to get the devices fabricated, and test them for any magnetic sensitivity. If they are sensitive that would open-up a new field for research - finding answers to the questions mentioned above; and mathematical modelling and computer simulation. The tests on the fabricated device, and any results obtained would not be a part of this thesis.

5. OP - AMP PARAMETERS AND TESTING

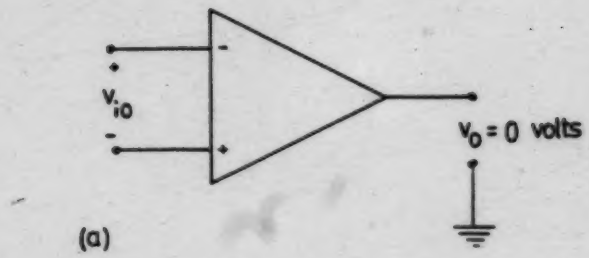
The main objective of this chapter is to put together a concise definition, and a method of testing the important parameters of an operational amplifier (not all the parameters are mentioned). The testing circuit given, and the component values mentioned are specifically suited to 'Internal Op-amps', and may not be suited for a general purpose Op-amp. For further information the reader should consult reference [9]. Also included is a small section on 'How to handle CMOS chips'.

5.1 Op-amp parameters and their measurement

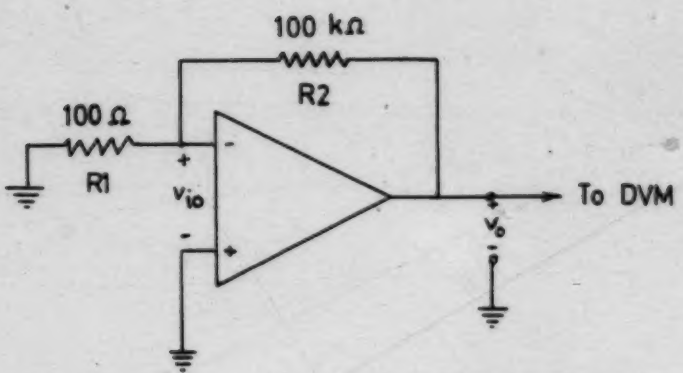
5.1.1 Input Offset Voltage

Definition The input offset voltage V_{IO} is that voltage which must be applied between the input terminals so as to force the output voltage to zero, as illustrated in figure 5.1 (a).

Measurement The circuit configuration of figure 5.1 (b) can be used to measure the input offset voltage of almost all types of Op-amps. The input offset voltage is read at the output magnified 1001 times, on a convenient scale of 1V to 1mV. If the input offset voltage is large enough to saturate the output (i.e., the magnitude of voltage V_o is almost equal to the supply voltage), then the resistor R2 should be reduced to, say, 10kΩ.



(a)



$$V_{io} = \left(\frac{R1}{R1 + R2}\right) V_o$$

(b)

Figure 5.1 (a) Pertaining to the definition of input offset voltage. (b) Circuit for measuring the input offset voltage

5.1.2 DC Open-Loop Gain

Definition The dc open-loop gain is the negative of the ratio of open-loop output voltage change to the differential input change at zero common-mode input voltage.

The gain defined this way is a positive number.

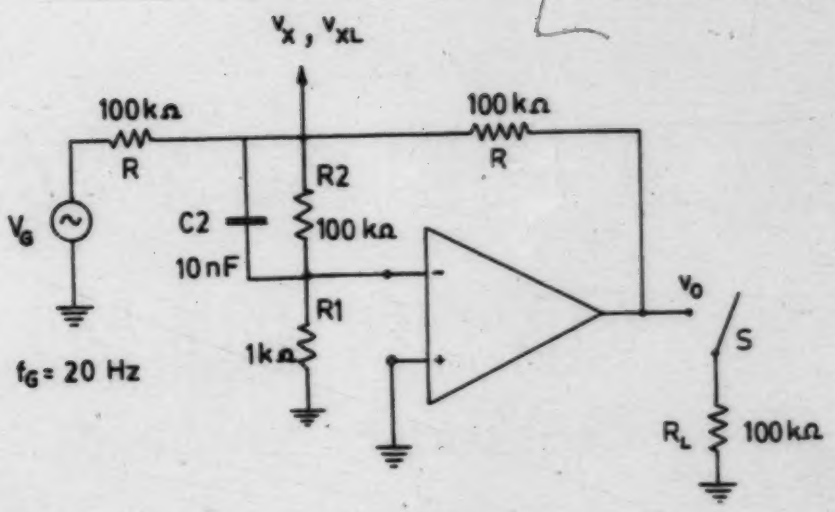
Measurement The circuit diagram is shown in figure 5.2 For an effective separation of the signal from offset, the dc open-loop gain A_o is measured at ac with a sine-wave excitation. The frequency of excitatin f_s should be lower than the first corner frequency, f_o. This condition can easily be checked : if the test frequency is slightly increased, the ratio of the readings on the two meters v_o and v_x should not change.

In the circuit elements R1, R2, and C2 act as a frequency-dependent voltage divider, providing feedback amplification and acting as an active low-pass filter with a gain of R2/(R1+1) ≅ 100, and a noise bandwidth 1/(4.C2.R2) = 250Hz. The signal voltage is enhanced and the wideband noise voltage is selectively suppressed.

5.1.3 Unity-Gain Frequency

Definition The unity-gain frequency is defined as that frequency f_t at which the open-loop gain gain is reduced to 1.

With respect to the frequency response plot of figure 5.3, unity-gain frequency is that frequency when the open-loop gain crosses the 0-dB line.



$$A_o = \left(\frac{R2}{R1} + 1\right)\frac{v_o}{v_x}$$

R_L used to determine output resistance R_o

Figure 5.2 Circuit for the measurement of dc open-loop gain

Measurement The circuit configuration of figure 5.2 can also be used for the point-by-point measurement of the Op-amp frequency response. As the frequency is increased, the value of the capacitor C2 should be reduced so that $1/(2\pi.C2.R2) >> f_c$ In most cases it is not necessary to search for the frequency at which the two voltmeter readings v_o, and v_x are equal. Instead it is sufficient to set f_c to a convenient value within one decade below the expected value of f_t, then rely on the -20 dB/decade roll-off (see figure 5.3) and calculate f_t from the voltmeters' readings using the equation

$$f_t = f_c[v_o/v_x] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.1)$$

5.1.4 Output Resistance

Definition The output resistance R_o is the internal resistance of the operational amplifier output with respect to ground.

Measurement The same circuit of figure 5.2 can be used for measuring output resistance R_o. The frequency of excitation f_c is set to be 1 kHz. Capacitor C_2 is chosen such that $1/(2\pi R_2C_2) >> 1$ kHz. The switch S is kept open and the value of voltage v_x corresponding to the output voltage v_o is noted. Then the switch S is closed, the amplitude of signal generated V_c is adjusted till v_o is the same as in the previous case. Then the voltage v_x with the load, called v_{xL}, is noted. The output resistance R_o can then be calculated by the relation

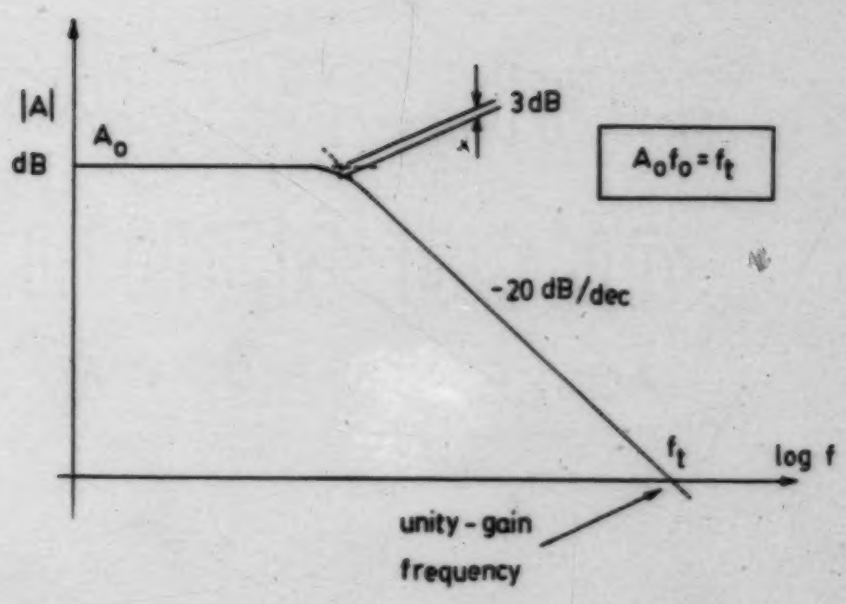


Figure 5.3 Definition of unity-gain frequency

$$R_o||R_L = R_L[(v_{xL}/v_x) - 1] \quad \text{.....(5.2)}$$

5.1.5 Common Mode Rejection Ratio (CMRR)

Definition The Common Mode Rejection Ratio CMRR is the ratio of the common-mode input voltage change to the differential input voltage change at zero output voltage without load.

Measurement The circuit of figure 5.4 can be used to measure the CMRR of a given Op-amp. The accuracy of measurement can be improved by keeping the output signal level of the Op-amp under test to be small. In order to maintain this condition, and to facilitate an easy measurement using a DVM an auxiliary Op-amp (μA 741) is used, as shown in figure 5.4.

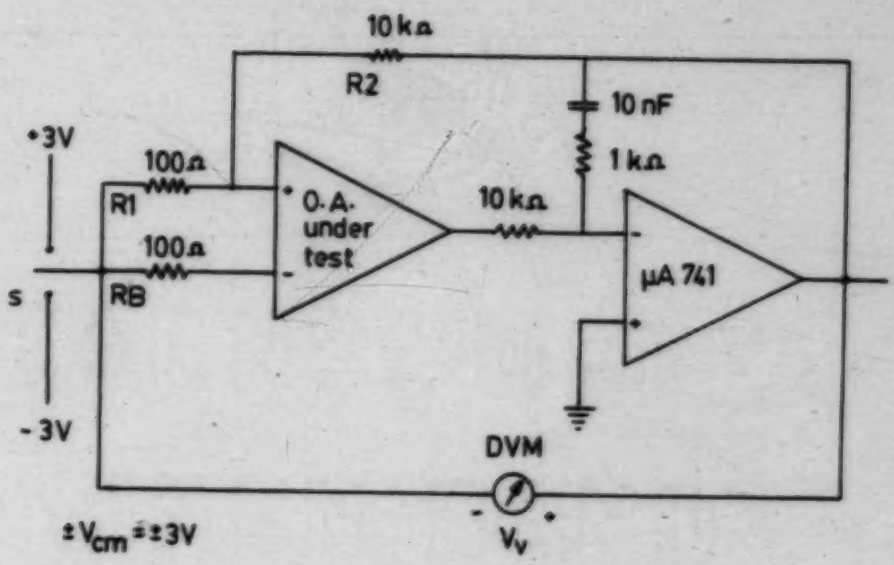
A compensation network is provided to ensure the stability of the network. The two-point measurement is carried out by reversing the switch S and noting the change in voltmeter reading Δv_v, which corresponds to the common-mode excitation within the limits $v_{cm} = \pm V_{cm}$. The dc CMRR is then calculated from the equation

$$CMRR = (R_2/R_1 + 1)\,[\Delta v_{cm}/\Delta v_v] \quad \text{.....(5.3)}$$

5.1.6 Power Supply Rejection Ratio, PSRR

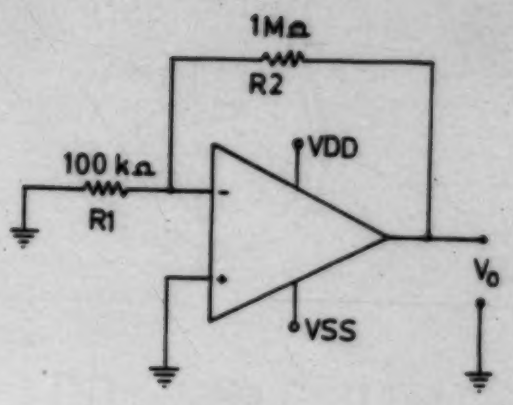
Definition Power Supply Rejection Ratio is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power supply voltages held constant.

Measurement The circuit setup is shown in figure 5.5. VDD is made equal to +5 volts, VSS is made equal to -5 volts, and



$$CMRR = \left(\frac{R2}{R1} \cdot 1\right) \frac{\Delta V_{cm}}{\Delta V_v}$$

Figure 5.4 Circuit for the measurement of Common Mode Rejection Ratio



$$V_{io} = \left(\frac{R1}{R1+R2}\right) V_o$$

$$PSRR = \frac{\Delta V_{io}}{\Delta VDD}$$

Figure 5.5 Circuit set-up for the measurement of Power Supply Rejection Ratio

the value of v_o is noted. Keeping VSS constant, VDD is reduced to +4 volts, and then to +6 volts; in each case the output voltage v_o is recorded. Then the input-referred offset voltage is calculated for each setting of VDD using the formula

$$V_{io} = [R_1/(R_1+R_2)].V_o \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.4)$$

Now we have a step of 2 volts in VDD (from +4 volts to +6 volts), and we know the corresponding input-referred offset voltages. From these, the PSRR can be calculated using the formula

$$PSRR = \Delta V_{io}/\Delta VDD \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.5)$$

The same thing can be repeated for VSS; VDD being kept constant at +5 volts.

PSRR has been found to be a function of frequency. In other words a frequency response can be plotted for PSRR. This can be easily done, using a function generator which gives a sine-wave with a dc offset, such as the HP 8111A (20 MHz) function generator. Instead of VDD, a sine-wave of 2 volts peak-to-peak floating on top of a dc offset of 5 volts is used. The frequency of the sine-wave is changed and for each setting the ac peak-to-peak value at the output is noted. Then the corresponding value at the input is determined using (5.4), and PSRR for each setting is calculated using (5.5). By repeating this procedure over the required frequency range a frequency response of PSRR can be plotted. A similar plot can be obtained for VSS also.

5.1.7 Slew Rate

Definition It is the time rate of change of the closed-loop amplifier output voltage under large-signal conditions.

Measurement The circuit set-up for the measurement of slew-rate is shown in figure 5.6. While making the measurement the output can be made to look like figure 5.6(b) by increasing the input amplitude and frequency. Once this kind of output is obtained, the output pulse amplitude, and times t_1 and t_2 are measured using a good CRO. Then the slew-rate is given by [(Pulse amplitude)/time t_1 or t_2]. It is common to specify the slower of the above two as the slew-rate of the Op-amp.

5.1.8 Quiescent Supply Current, and Power Dissipation

Definition

Quiescent Supply Current, IDD (ISS), is the current drawn from the drain (source) supply, with both the input terminals at ground potential and without any load.

Power Dissipation

$$\text{Power Dissipation} = VDD.IDD + [|VSS|.|ISS|]$$

where

VDD is the drain supply volatge, and

VSS is the source supply voltage.

Measurement The circuit set-up is shown in figure 5.7 If the Op-amp has only two supply leads, it is sufficient to check the supply current of one of them only. If there is a ground terminal as well, both IDD and ISS should be measured.

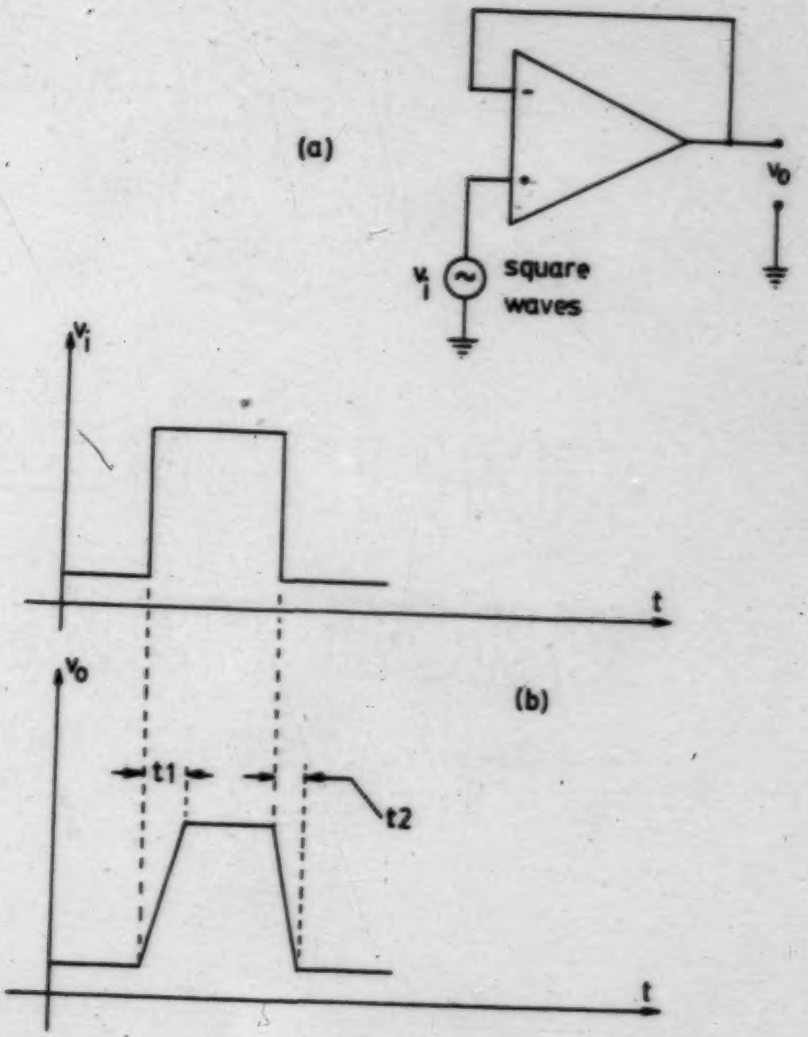


Figure 5.6 (a) Circuit for the measurement of slew-rate, (b) input and output waveforms

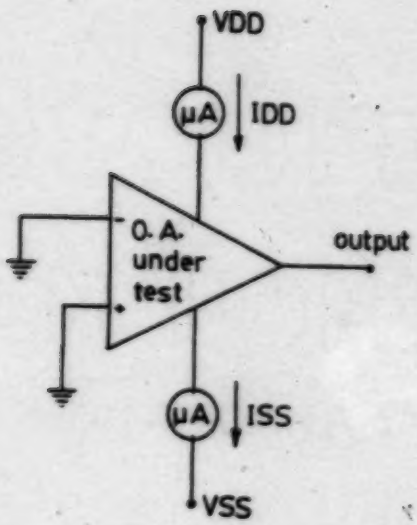


Figure 5.7 Circuit set-up for Quiescent Supply Current measurement

5.2 Handling CMOS Chips

The thickness of silicon dioxide layer that separates the gate from the conduction channel in any MOSFET is usually of the order of 850 Angstroms. The dielectric break-down voltage of amorphous silicon dioxide for most IC applications is in the range of 6E+6 volts/cm to 9E+6 volts/cm. This means a potential of about 51 volts to 77 volts can cause breakdown of the silicon dioxide layer, and destroy the transistor. Such levels of potential can easily be built-up because of static electricity. Therefore one has to be very careful in dealing with CMOS IC chips.

It is very desirable to have gate input protection circuits incorporated into the chip. Figure 5.8 shows one of the gate protection circuit diagram. As the input potential exceeds VDD, diodes D1 and D2 conduct, thereby protecting the gate. Note that the resistor R does not affect the performance of the transistor since the gate current is extremely small, and R is of the order of few kilo ohms.

If no gate protection is provided one has to be very careful in handling the chips. Some useful hints are outlined below

3. The test-circuit should be wire-wrapped on a perforated board. All the pins of the socket that holds the IC chip should normally remain shorted by a conductive foam. This conductive foam has a desirable property that it has a resistance of about 20 kilo ohms/cm. Because of this, power could be turned on with the conducting foam

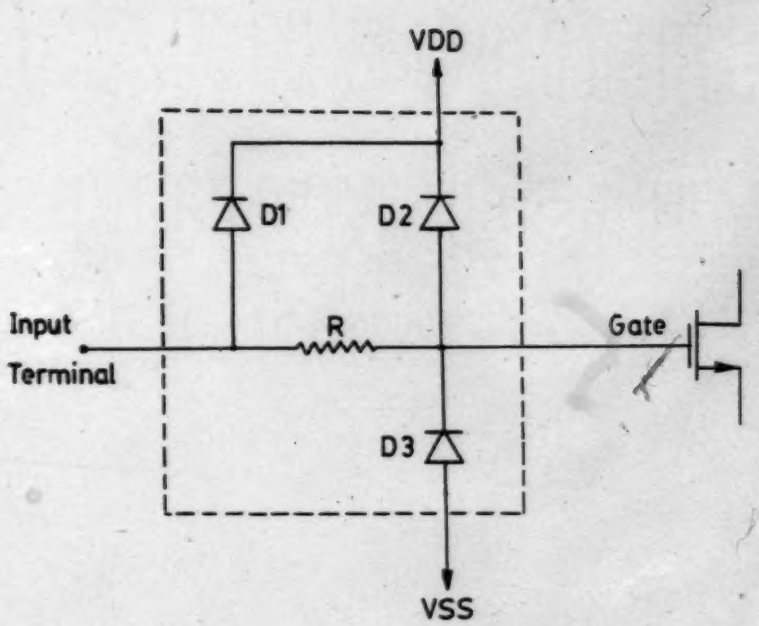


Figure 5.8 Gate input protection circuit

in its intended place, without shorting the power supply. Then the conducting foam is slowly peeled-off from the wire-wrap socket and the required experiment can be carried out. After the experiment is over, the conductive foam is inserted back, and power can be switched off.

4. The person conducting the test should be standing barefoot on a conducting mat. If that is not possible, he should be seated on a metal stool, with his feet resting on a metal footrest, which should be connected to the system ground. He should be wearing conducting wrist-straps that are wired to the system ground. Also he should preferably wear cotton clothing.
5. Signals should not be applied to the inputs while the device power supply is off.
6. There is a high possibility of the device being damaged when transferring from its anti-static storage tube to the wire-wrapped test-circuit socket. Since higher humidity levels tend to reduce the magnitude of the static voltage generated, this initial transfer should be done in a place of high humidity (e.g., any bathroom, immediately after a hot shower). The conducting foam stuck at the back of the socket will prevent static voltage build-up when the chip is not in use. In spite of all these precautions it is possible to damage a few chips before the successful completion of testing.

6. RESULTS AND CONCLUSION

The three Op-amps described in this thesis were fabricated using Northern Telecom CMOS-1B process. The results obtained from tests conducted on the three Op-amps are summarized in the first section. These results are discussed in the second section. This is followed by the third section where some general conclusions drawn from the work reported in this thesis are outlined.

6.1 Results

The results obtained by testing the fabricated Op-amps are given in the following pages. All the parameters mentioned are defined in chapter 5. Also the method of measurement and details of the test circuit are given there. It would be beneficial to go through the discussion section also since some oddities encountered while testing are explained in that section.

Table 6.1 Results of measurements conducted on Op-amp # 1

Input offset voltage	64 mV (see discussioin)
DC open-loop gain	3100 (69.8 dB)
Unity-gain frequency	3 MHz
Output resistance	85.2 K Ohms
CMRR	40.2 dB
PSRR on VDD on VSS	-38.19 dB -45.93 dB
Slew rate	1.35 V / micro sec -30 V / micro sec
Quiescent supply current	IDD:42.5 micro amps ISS:42.5 micro amps (see discussion)
Power dissipation	425 micro watts (see discussion)

Table 6.2 Results of measurements conducted on Op-amp # 2

Input offset voltage	0.6 mV
DC open-loop gain	2960 (69.4dB)
Unity-gain frequency	2.5 MHz
Output resistance	27.3 K Ohms
CMRR	73.8 dB
PSRR on VDD on VSS	-50 dB -45.43 dB
Slew rate	5.2 V/micro sec -3.1 V/micro sec
Quiescent supply current	IDD:153 micro amps ISS:145 micro amps
Power dissipation	1.488 mW

Table 6.3 Results of measurements conducted on Op-amp # 3

Input offset voltage	4.9 mV
DC open-loop gain	5200 (74.3 dB)
Unity-gain frequency	see discussion
Output resistance	13.16 K Ohms
CMRR	51.36 dB
PSRR on VDD on VSS	-80 dB -74.6 dB
Slew rate	0.8 V / micro sec -8.0 V / micro sec
Quiescent supply current	IDD: 122 micro amps ISS: 120 micro amps
Power dissipation	1.21 mW

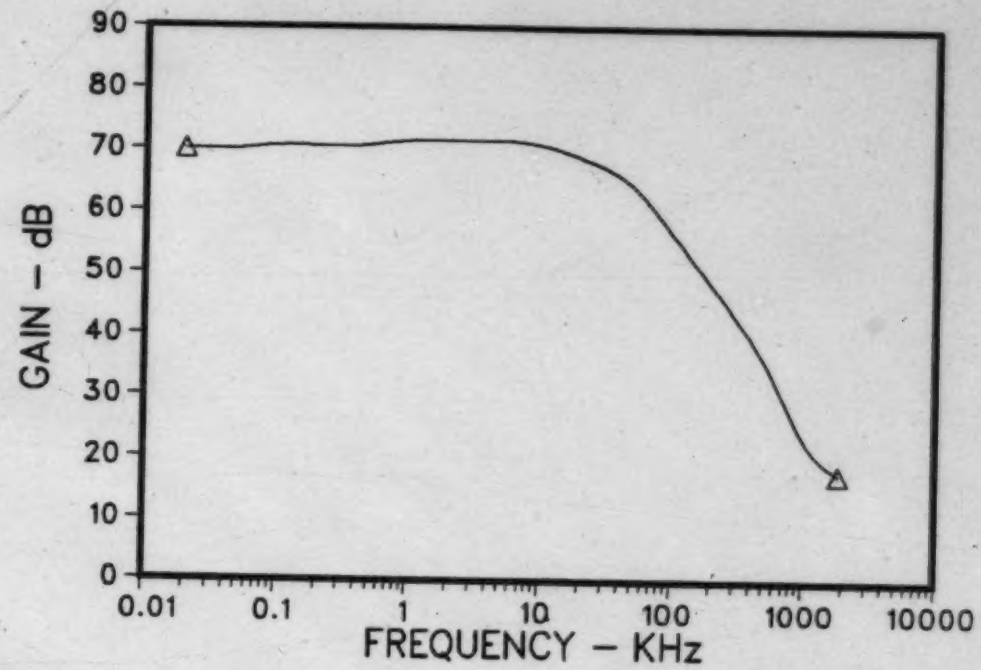


Figure 6.1 Open-loop frequency response for Op-amp # 1

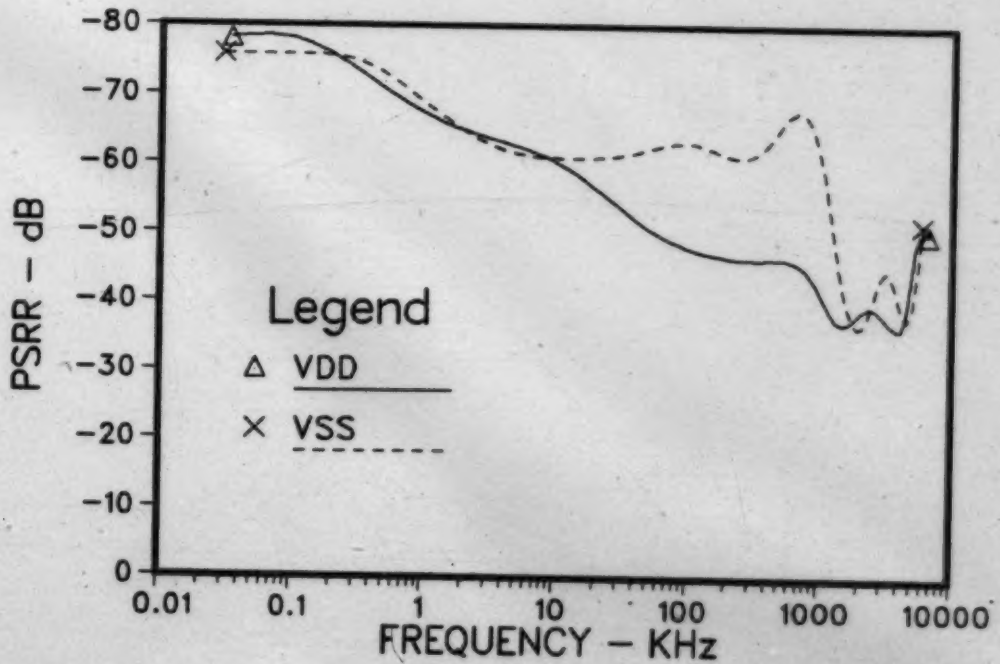


Figure 6.2 PSRR versus frequency for Op-amp # 1

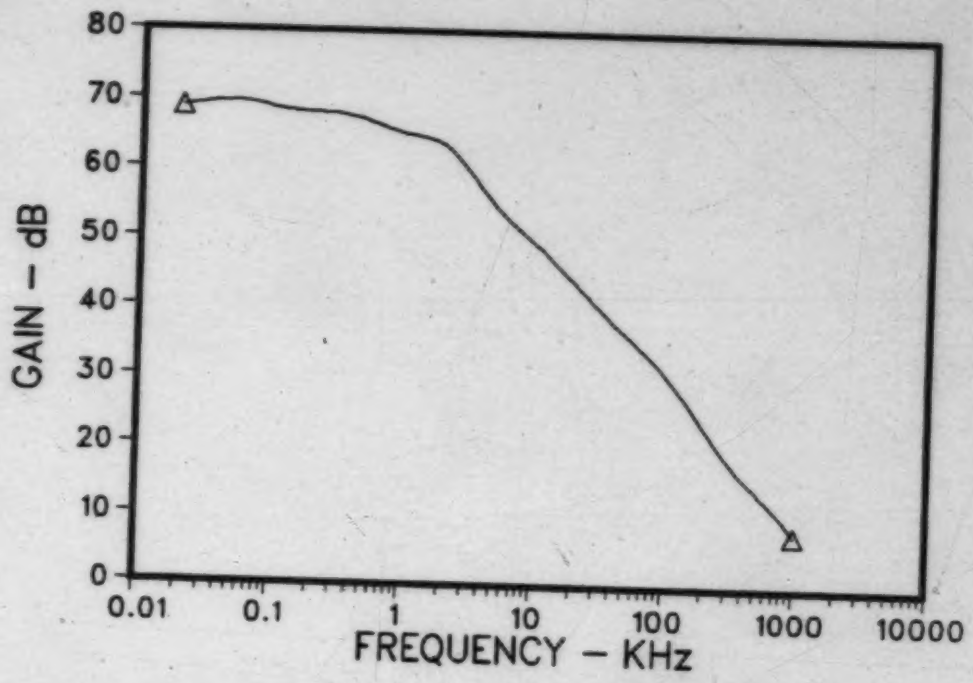


Figure 6.3 Open-loop frequency response for Op-amp # 2

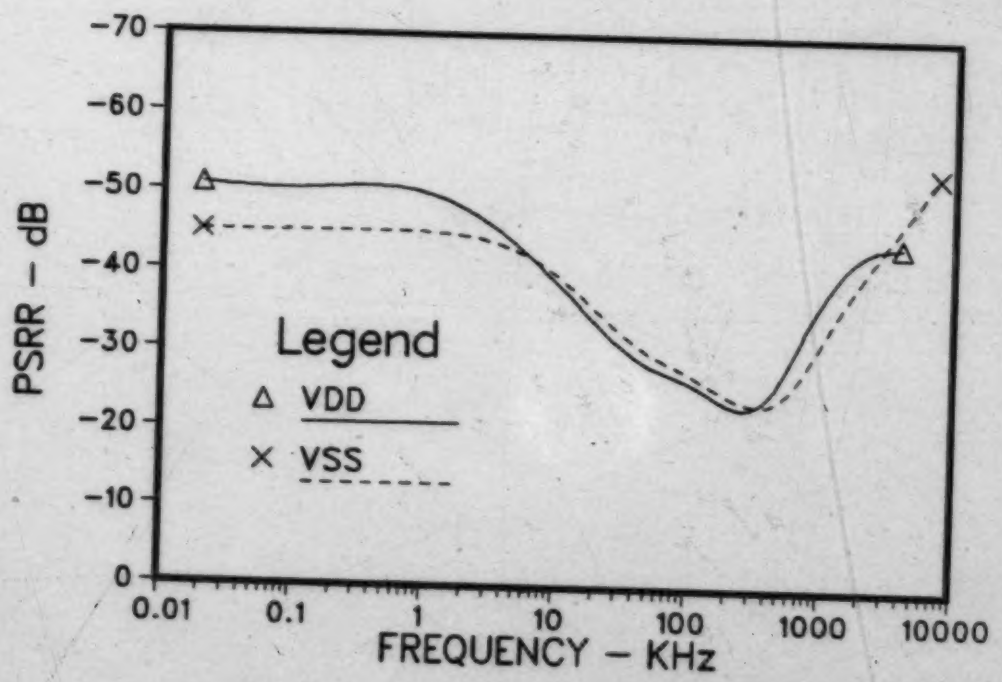


Figure 6.4 PSRR versus frequency for Op-amp # 2

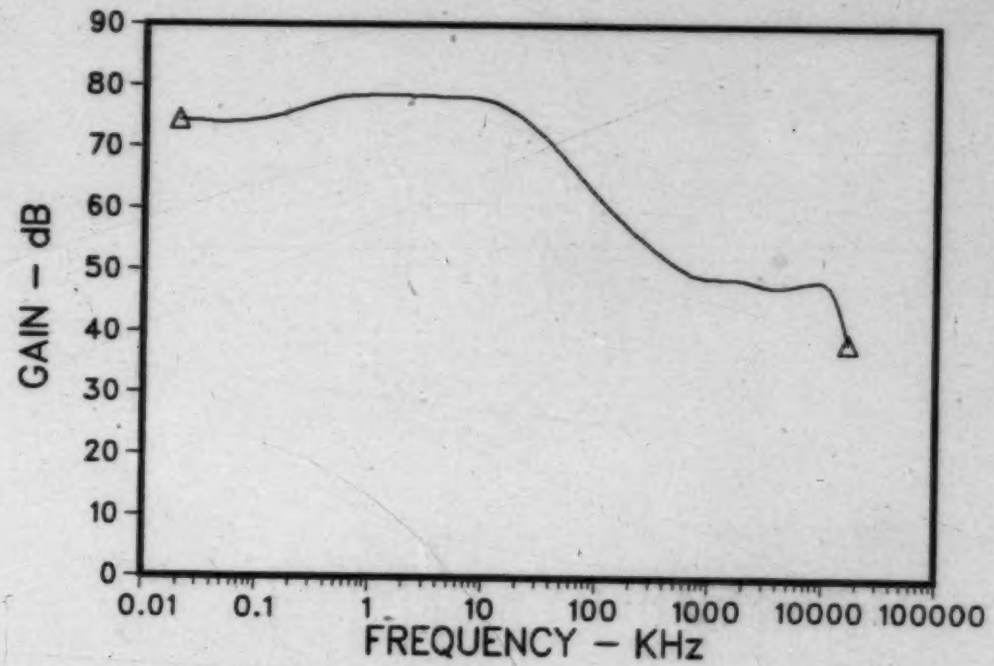


Figure 6.5 Open-loop frequency response for Op-amp # 3

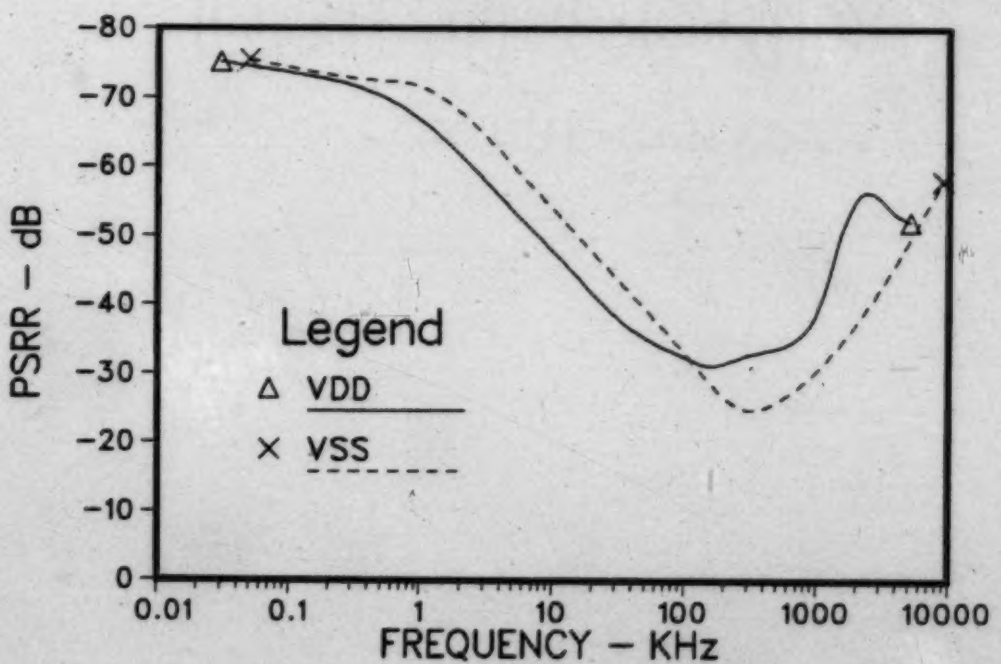
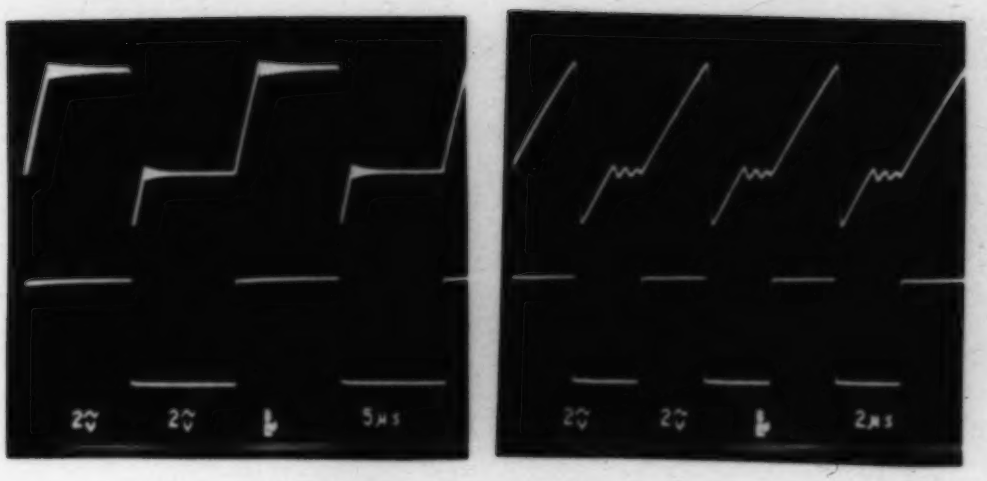
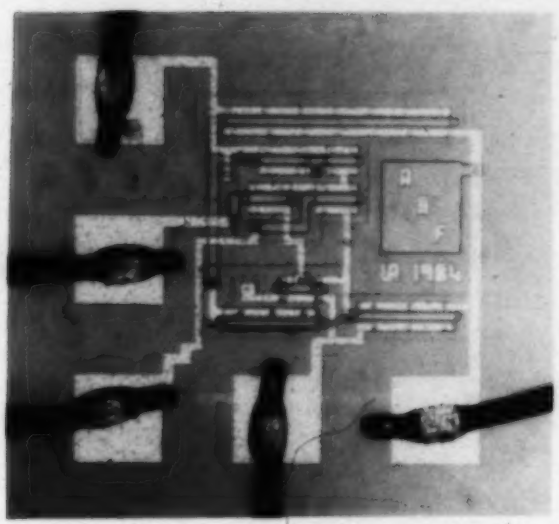


Figure 6.6 PSRR versus frequency for Op-amp # 3

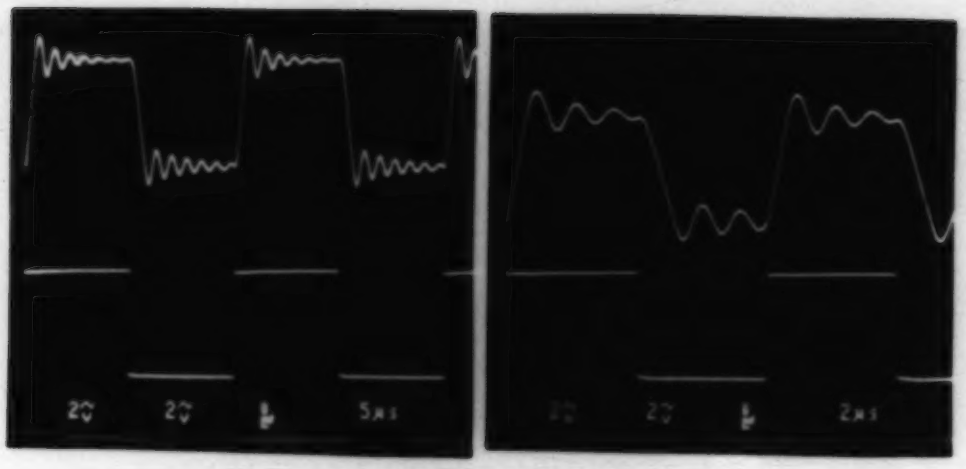


(a) (b)

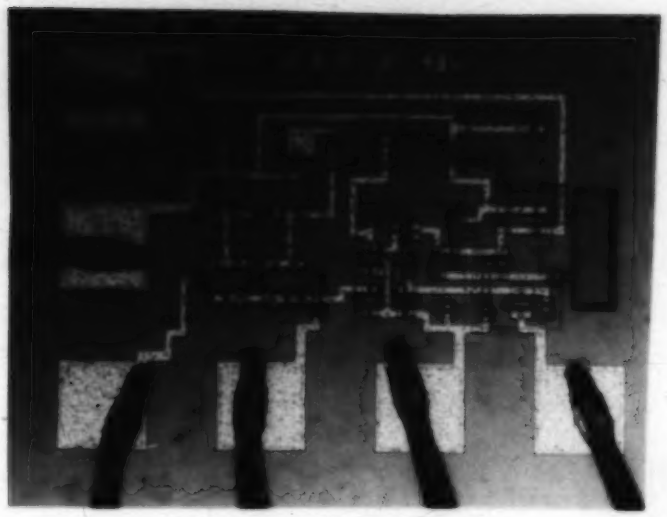


(c)

Plate 6.1 Op-amp # 1 (a) Step response at 50kHz (b) Step response showing slew-rate limitations (frequency = 200kHz) (c) Photomicrograph



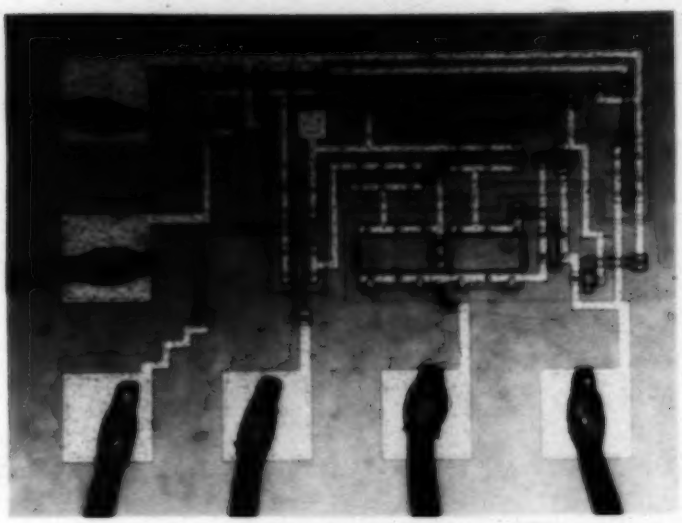
(a) (b)



(c)

Plate 6.2 Op-amp # 2 (a) Step response at 50kHz (b) Step response showing slew-rate limitations (frequency = 100kHz) (c) Photomicrograph

(a) (b)



(c)

Plate 6.3 Op-amp # 3 (a) Step response at 50kHz (b) Step response showing slew-rate limitations (frequency = 100kHz) (c) Photomicrograph

6.2 Discussion

In this section the results obtained from the tests performed on the fabricated Op-amps are analyzed. They are compared with the results obtained from the simulation and a possible explanation is given for any discrepancies that might exist.

6.2.1 Op-amp # 1

We will start with the measured results of Op-amp # 1, given in table 6.1. The input offset voltage of 65 mV is high. It could be because of bad layout or bad processing or something else. Since Op-amps 2 and 3 have very reasonable offset voltages, bad processing may not be the reason for this high offset voltage. Whether it is because of bad layout or something else is hard to say.

During the course of measurements it was observed that the input offset voltage sometimes changed suddenly by a large amount. For instance on the first day of measurements with Op-amp # 1, the input offset voltage recorded was 65 mV. A week later when the measurements were resumed, the offset was found to be 1.08 volts which is totally unacceptable. Such drastic variation of input offset voltage was also observed with Op-amps # 2, and 3.

Comparing the next two parameters, namely DC open-loop gain and unity-gain frequency with the simulation results given in table 3.3 we find that both of them are slightly higher than that of simulation results, and are acceptable

values. The output resistance of 85 kΩ is not high, considering that these Op-amps do not have an output stage. CMRR and PSRR are comparatively low.

A total of four chips were fabricated for each Op-amp. When the first Op-amp was received, over-enthusiasm and lack of protection circuitry resulted in the destruction of three chips, leaving only one chip for testing. At the time of measurement of supply current and power dissipation, the input offset was 1.08 volts. This clearly means that the second stage was drawing very little current. The recorded current of 42.5 micro amperes is almost equal to the sum of the simulated current through M5 (17μA) and M8 (24.3μA) [see table 3.3 and figure 3.1]

6.2.2 Op-amp # 2

Refer to figure 3.3 for the circuit diagram, table 3.5 for simulation results, and table 6.2 for test results. From table 6.2 we see that the offset voltage is 0.6 mV, which is quite acceptable. The open-loop gain falls short of the simulation results, while the unity-gain frequency is slightly above that of the simulation result. Output resistance of 27 KΩ is quite low. CMRR of 73 dB is good, while the PSRR is only marginal. The slew rate and supply current are slightly higher than the simulation values. In all, except for open-loop gain and PSRR, other parameters are equal to or better than expected values.

6.2.3 Op-amp # 3

The simulated and measured parameter values are listed in tables 3.9 and 6.3 respectively. The offset voltage of 4.9 mV is typical for these kind of Op-amps. The open-loop gain is slightly less than the simulated value. To comment on the unity-gain frequency we refer the reader to the open-loop frequency response given in figure 6.5. Notice that after rolling off for some time at 20 dB per decade the open-loop frequency response becomes flat. This means that there is a zero encountered and this must be avoided to insure stability. As discussed in the frequency compensation section, this zero can be pushed to higher frequency by making the value of the series resistor R_z equal to the transconductance of the second stage. It appears as though the value of the resistance is not sufficient. The solution to this problem is to increase the length of transistors MC1 and MC2 of figure 3.6.

Output resistance of 13 KΩ is the lowest of the three Op-amps tested. CMRR of 50 dB is marginally acceptable, while, PSRR is good. Positive slew-rate is slightly less than expected value. Supply currents and power dissipation are almost equal to the expected values. From the above comparison the only place where we have serious disagreement is with the unity-gain frequency, for which a solution has been suggested.

It may be mentioned here that all the simulation were carried out with a load resistance of 5 MΩ and a load

capacitance of 15 pF. These are typical values that will be encountered in the intended area of application of these internal Op-amps. But in the actual measurement the loading was more than that used for simulation. The CRO presented a load of 1 MΩ in parallel with 15 pF of capacitance. Including the capacitance of the probes, wires, and the SK-10 breadboard, the total capacitance may be put at about 25 to 35 pF. Considering this, it may be said that the performance of these Op-amps under actual usage as part of a more complex circuit could be better than what is given in the results section.

6.3 Conclusion

Three different internal Op-amp circuits were designed, fabricated using the Northern Telecom CMOS-1B process, and tested. Each of the circuit was simulated using SPICE to determine the optimum device sizes, and performance parameters. The simulation program SPICE was found to be an useful tool for designing Op-amps. But it requires a lot of computer time, and fails to converge quite frequently, which can be very frustrating.

Some form of computer aided layout and design rule checking system becomes a must if one has to try a few layouts. Layout preparation by hand is very time consuming and prone to errors.

In the Op-amps described in this thesis no gate input protection circuitry was used. This resulted in the

destruction of many chips. Considering the limitation on the number of prototypes that can be fabricated for testing, it was found desirable to incorporate input gate protection.

The results obtained from the tests conducted on the fabricated chips are in good agreement with the computer simulation results. It was observed that the input offset voltage exhibited a tendency to change abruptly from a value of few millivolts to several hundreds of millivolts in a couple of days, for reasons that are not very clear. In Op-amp # 2 and Op-amp # 3, transistors were used to realize the nulling resistor required in series with compensating capacitor. This method worked well for Op-amp # 2, and needs some modifications for Op-amp # 3.

At the time of writing this thesis the modified Op-amp for sensing magnetic fields was not received from Northern Telecom. Hence no experimental results are given on the magnetic field sensor.

And finally it is hoped that the work reported in this thesis will be useful for further research work in CMOS analog circuitry using the Northern Telecom fabrication facilities.

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APPENDIX A

The CIF short names and associated colours used in the plots in this thesis are listed below. The CALMA levels associated with the various CMOS layers are also included. These levels correspond to NT CMOS-1B technology and, for this process, levels 4,7, and 11 denote exclusion regions while all other levels describe inclusion regions.

CALMA LEVEL	FUNCTION	CIF CODE	PLOTTING COLOR
1	P-Well	LCPW;	Green (long dotted)
2	Device Well	LCF;	Blue solid
3	P Guard	LCPG;	Blue (long dotted)
4	N Guard	LCNG;	Red (long dotted)
5	Cap. Poly	LCCP;	Red (medium dotted)
6	Poly	LCP;	Red solid
7	N+	LCNP;	Red (small dotted)
8	P+	LCPP;	Blue (small dotted)
9	Contact	LCC;	Green (small dotted)
10	Metal	LCM;	Green solid
11	Glass	LCG;	Blue (medium dotted)

AHF PROGRAM FOR THE LAYOUT OF OP-AMP # 1:

```
{Layout description for simple Op-amp}
chip opampone;
symbol opamp;
   begin
      lcpw; poly 178,178 & 178,280 &380,280 & 380,240
              & 560,240 & 560,178;

      lcf;  box 190,195 & 200,205; {dev well, M9}
            box 200,195 & 360,203;
            box 360,195 & 370,205;
            box 400,190 & 540,230;  {M6}
            box 235,240 & 255,255;  {p-well}
            box 290,230 & 300,266;  {M3}
            box 340,230 & 350,266;  {M4}
            box 245,355 & 305,397;  {M1}
            box 340,355 & 400,397;  {M2}
            box 260,410 & 326.7,450;  {M8}
            box 355.5,410 & 400,450;  {M5}
            box 210,465 & 530,505;  {M7}
            box 210,400 & 220,420;  {subst}
      lcpg; poly 173,173 & 173,285 & 385,285 & 385,245
            & 565,245 & 565,173;

      lcng; poly 170,170 & 170,288 & 388,288 & 388,248
            & 568, 248 & 568, 170;

      lccp; box 378,308 & 430,322;   {cap poly}
            box 430,296 & 550,433;

      lcp;  box 210,190 & 344.4,220; {poly, M9}
            box 380,205 & 392,218;   {M6}
            box 392,205 & 546,215;
            box 188,248 & 202,490;   {M9-M7}
            box 202,480 & 540,490;   {M7}
            box 202,425 & 406,435;   {M8-M5}
            box 334,408 & 346,425;
            box 218,338 & 232,370;   {M1}
            box 218,370 & 312,382;
            box 320,370 & 406,382;   {M2}
            box 248,328 & 320,342;
            box 320,328 & 330,370;
            box 284,243 & 356,253;   {M3-M4}
            box 310,253 & 330,270;
            box 434,300 & 546,429;
            box 546,410 & 575,425;   {capacitor}
```

```
lcnp; box 225,230 & 265,265;
      poly 170,525 & 555,525 & 555,450 &
           420,450 & 420,335 & 355,335 &
           355,310 & 230,310 & 230,450 & 170,450;

lcpp; box 230,235 & 260,260;
      poly 175,520 & 550,520 & 550,455 &
           415,455 & 415,340 & 350,340 &
           350,315 & 235,315 & 235,455 & 175,455;

lcc;  box 192,197 & 197,202;   {M9}
      box 362,197 & 367,202;
      box 422,192 & 427,197;   {M6}
      box 472,192 & 477,197;
      box 522,192 & 527,197;
      box 383,208 & 388,213;
      box 232,212 & 238,217;   {M9}
      box 277,212 & 283,217;
      box 322,212 & 328,217;
      box 422,223 & 427,228;   {M6}
      box 472,223 & 477,228;
      box 522,223 & 527,228;
      box 292,232 & 298,237;   {M3}
      box 292,258 & 298,263;
      box 342,232 & 348,237;   {M4}
      box 342,258 & 348,263;
      box 317,258 & 322,263;   {M3}
      box 242,245 & 248,250;   {p-well}
      box 192,252 & 198,258;   {M9-M7}

      box 212,407 & 218,413;   {substrate}
      box 222,342 & 228,348;   {M1}
      box 252,332 & 258,338;   {M2}
      box 382,312 & 388,318;   {cap}
      box 564,414 & 570,420;
      box 337,412 & 343,418;   {M8-M5}

      box 255,357 & 260,362;   {M1}
      box 255,390 & 260,395;
      box 290,357 & 295,362;
      box 290,390 & 295,395;

      box 350,357 & 355,362;   {M2}
      box 350,390 & 355,395;
      box 390,390 & 395,395;
      box 390,357 & 395,362;

      box 272,412 & 277,417;   {M8}
      box 272,442 & 277,447;
      box 312,412 & 317,417;
      box 312,442 & 317,447;

      box 362,412 & 367,417;   {M5}
```

```
        box 362,442 & 367,447;
        box 390,412 & 395,417;
        box 390,442 & 395,447;

        box 222,467 & 227,472;    {M7}
        box 215,498 & 220,503;
        box 272,467 & 277,472;
        box 265,498 & 270,503;
        box 322,467 & 327,472;
        box 315,498 & 320,503;
        box 372,467 & 377,472;
        box 365,498 & 370,503;
        box 422,467 & 427,472;
        box 415,498 & 420,503;
        box 472,467 & 477,472;
        box 465,498 & 470,503;
        box 522,467 & 527,472;
        box 515,498 & 520,503;

lcm;    box 0,0 & 125,125;        {input2}
        box 125,110 & 140,155;
        box 140,140 & 165,155;
        box 150,155 & 165,170;
        box 165,160 & 180,170;
        box 170,170 & 180,320;
        box 180,310 & 260,320;
        box 250,320 & 260,340;

        box   0,225 & 125,350;    {input1}
        box 125,335 & 230,350;

        box   0,450 & 125,575;    {VDD}
        box 125,560 & 200,575;
        box 190,450 & 200,560;
        box 190,440 & 400,450;
        box 210,400 & 220,440;
        box 200,495 & 530,505;

        box 225,  0 & 350,125;    {VSS}
        box 335,125 & 350,170;
        box 335,170 & 410,180;
        box 400,180 & 410,190;
        box 400,190 & 535,200;
        box 360,180 & 370,240;
        box 255,230 & 360,240;
        box 235,230 & 255,255;

        box 450,  0 & 575,125;    {output}
        box 560,125 & 575,475;
        box 210,465 & 560,475;
        box 405,220 & 560,230;

        box 190,195 & 200,260;    {M9-M7}
        box 200,210 & 340,220;
```

```
                box 290,256 & 315,266;    {M3-M1}
                box 315,256 & 325,320;
                box 295,310 & 315,320;
                box 295,320 & 305,355;
                box 245,355 & 305,365;

                box 380,205 & 390,355;    {M6-M4-M2}
                box 340,355 & 400,365;
                box 340,256 & 380,266;

                box 245,387 & 400,397;    {M1-M2-M5}
                box 375,397 & 385,410;
                box 355.5,410 & 400,420;

                box 260,410 & 345,420;    {M8}

        lcg;    box 6,6 & 119,119;        {pads}
                box 231,6 & 344,119;
                box 456,6 & 569,119;
                box 6,231 & 119,344;
                box 6,456 & 119,569;
end;
symbol aa;
   begin
      lcm;      box 0,0 & 5,25;
                box 10,0 & 15,25;
                box 5,5 & 10,10;
                box 5,20 & 10,25;
   end;

symbol ss;
   begin
      lcm;      box 0,0 & 5,7;
                box 5,0 & 15,5;
                box 5,0 & 15,5;
                box 10,5 & 15,15;
                box 5,10 & 10,15;
                box 0,10 &  5,20;
                box 0,20 & 10,25;
                box 10,18 & 15,25;
end;

symbol ff;
   begin
      lcm;      box 0,0 & 5,25;
                box 5,10 & 13,15;
                box 5,20 & 15,25;
   end;

symbol uofa;
   begin
      lcm;      box 0,5 & 5,25;
                box 0,0 & 15,5;
```

```
            box 10,5 & 15,20;
            box 10,20 & 25,25;
            box 20,0 & 25,20;
            box 15,8 & 20,13;
   end;

symbol year;
   begin
      lcm;  box 0,0 & 5,25;
            box 10,10 & 15,25;
            box 10,10 & 15,25;
            box 20, 0 & 25,25;
            box 15,10 & 20,15;
            box 15,20 & 20,25;
            box 30, 0 & 35,25;
            box 40, 0 & 45,25;
            box 35, 0 & 40, 5;
            box 35,10 & 40,15;
            box 35,20 & 40,25;
            box 50, 5 & 55,25;
            box 55, 5 & 60,10;
            box 60,0 & 65,15;
   end;

begin
   opamp;
   aa t (460,395);
   ss t (485,355);
   ff t (510,315);
   uofa t (434,260);
   year t (481,260);
end.
```

AHF PROGRAM FOR OP-AMP # 2

```
            {Layout description for N-Opamp}
chip opamptwo;

  symbol cnt;
     begin
         lcc;    box 0, 0 & 5, 5;
     end;

  symbol iopad;
     begin
         lcm;    box 0, 0 & 125, 125;
         lcg;    box 6, 6 & 119, 119;
     end;


symbol aa;
   begin
      lcm;  box 0,0 & 5,25;
            box 10,0 & 15,25;
            box 5,5 & 10,10;
            box 5,20 & 10,25;
   end;

symbol ss;
   begin
      lcm;  box 0,0 & 5,7;
            box 5,0 & 15,5;
            box 5,0 & 15,5;
            box 10,5 & 15,15;
            box 5,10 & 10,15;
            box 0,10 &  5,20;
            box 0,20 & 10,25;
            box 10,18 & 15,25;
end;

symbol ff;
   begin
      lcm;  box 0,0 & 5,25;
            box 5,10 & 13,15;
            box 5,20 & 15,25;
   end;

symbol uofa;
   begin
      lcm;  box 0,5 & 5,25;
            box 0,0 & 15,5;
            box 10,5 & 15,20;
            box 10,20 & 25,25;
```

```
            box 20,0 & 25,20;
            box 15,8 & 20,13;
   end;

symbol year;
   begin
      lcm;  box 0,0 & 5,25;
            box 10,10 & 15,25;
            box 10,10 & 15,25;
            box 20, 0 & 25,25;
            box 15,10 & 20,15;
            box 15,20 & 20,25;
            box 30, 0 & 35,25;
            box 40, 0 & 45,25;
            box 35, 0 & 40, 5;
            box 35,10 & 40,15;
            box 35,20 & 40,25;
            box 50, 5 & 55,25;
            box 55, 5 & 60,10;
            box 60,0 & 65,15;
   end;

  symbol opamp;
     begin
        lcpw;  box  180, 180  & 380, 290;
               box  420, 180  & 575, 350;
               box  420, 390  & 575, 470;

        lcf;   box  210, 200  & 266, 270;  {m1}
               box  290, 200  & 346, 270;  {m2}
               box  210, 330  & 259, 395;  {m3}
               box  300, 330  & 349, 395;  {m4}
               box  430, 190  & 451, 235;  {m5}
               box  445, 420  & 465, 450;  {m6-S}
               box  465, 431  & 550, 440;  {m6-Tr}
               box  550, 425  & 560, 445;  {m6-D}
               box  430, 250  & 451, 295;  {m7}
               box  620, 310  & 689, 350;  {m8}
               box  470, 300  & 510, 325;  {m9}
               box  640, 190  & 671, 235;  {mB1}
               box  480, 190  & 501, 235;  {mB2}
               box  530, 245  & 545, 290;  {mC1}
               box  620, 245  & 635, 290;  {mC2}
               box  215, 435  & 245, 465;
               box  540, 190  & 560, 210;
               box  655, 445  & 685, 475;

        lcpg;  box  174, 174  & 386, 296;
               box  414, 174  & 581, 356;
               box  414, 384  & 581, 476;

        lcng;  box  170, 170  & 390, 300;
               box  410, 170  & 585, 360;
               box  410, 380  & 585, 480;
```

```
lccp;   box   726, 205  & 784, 374;
        box   690, 240  & 710, 260;
        box   710, 245  & 726, 255;

lcp;    box   190, 227  & 272, 253;   {m1}
        box   284, 227  & 358, 253;   {m2}
        box   358, 188  & 372, 253;   {m2}
        box   200, 345  & 360, 380;   {m3, m4}
        box   270, 325  & 290, 345;   {m3}
        box   424, 206  & 510, 220;   {m5, mB2}
        box   460, 220  & 470, 266;   {m5 to m7}
        box   424, 266  & 488, 280;   {m5 - m7}
        box   488, 244  & 502, 280;   {m5 - m7}
        box   375, 430  & 395, 450;   {m6, m8 &cap}
        box   380, 400  & 390, 430;   {m6, m8 &cap}
        box   390, 400  & 500, 410;   {m6, m8 &cap}
        box   476, 410  & 540, 450;   {m6, m8 &cap}
        box   540, 410  & 630, 420;   {m6, m8 &cap}
        box   620, 370  & 630, 410;   {m6, m8 &cap}
        box   630, 370  & 715, 380;   {m6, m8 &cap}
        box   705, 335  & 715, 370;   {**}
        box   614, 325  & 730, 335;   {**}
        box   730, 209  & 780, 370;   {**}

        box   430, 320  & 450, 340;   {m9 &connection}
        box   450, 330  & 495, 340;
        box   485, 294  & 495, 330;

        box   524, 260  & 565, 273;   {mC1}
        box   555, 273  & 565, 320;
        box   550, 320  & 570, 340;

        box   598, 185  & 615, 205;   {mC2}
        box   600, 205  & 610, 260;
        box   600, 260  & 641, 273;

        box   630, 205  & 680, 215;   {mB1}
        box   680, 190  & 700, 220;

lcnp;   box   248, 193  & 262, 210;   {m1}
        box   296, 193  & 310, 210;   {m2}
        box   435, 425  & 455, 445;   {m6}
        box   543, 193  & 557, 207;
        poly  185, 310  & 185, 415  & 365, 415  &
              365, 395  & 375, 395  & 375, 310;
        poly  585, 170  & 585, 360  &
              698, 360  & 698, 285  &
              685, 285  & 685, 235  &
              715, 235  & 715, 170;

lcpp;   box   248, 196  & 262, 210;   {m1}
        box   296, 196  & 310, 210;   {m2}
        box   543, 193  & 557, 207;
```

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        box  440, 425  & 455, 445;

        poly 190, 315  & 190, 410  &
             360, 410  & 360, 390  &
             370, 390  & 370, 315;

        poly 590, 175  & 590, 355  &
             695, 355  & 695, 290  &
             680, 290  & 680, 230  &
             710, 230  & 710, 175;

lcc;    box  253, 204  & 258, 216;  {m1}
        box  300, 204  & 305, 216;  {m2}
        box  228, 445  & 233, 455;  {left}
        box  665, 458  & 675, 463;  {right}
        box  449, 433  & 461, 438;  {m6}

        cnt t 213, 213;
        cnt t 233, 213;
        cnt t 320, 213;
        cnt t 338, 213;
        cnt t 363, 192;
        cnt t 194, 237;
        cnt t 220, 263;
        cnt t 250, 263;
        cnt t 303, 263;
        cnt t 330, 263;

        cnt t 220, 333;             {m3 & m4}
        cnt t 245, 333;
        cnt t 277, 333;
        cnt t 313, 333;
        cnt t 335, 333;
        cnt t 220, 387;
        cnt t 245, 387;
        cnt t 313, 387;
        cnt t 335, 387;

        cnt t 383, 437;             {m6}
        cnt t 552, 433;

        cnt t 438, 193;             {m5}
        cnt t 438, 228;

        cnt t 438, 253;             {m7}
        cnt t 438, 288;
        cnt t 438, 328;

        cnt t 473, 310;             {m9}
        cnt t 503, 310;
        cnt t 493, 247;             {mB2}
        cnt t 488, 228;
        cnt t 488, 193;
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```
            cnt t 535, 282;              {mC1}
            cnt t 535, 248;              {mC1}
            cnt t 557, 328;
            cnt t 547, 197;              {p-well}

            cnt t 603, 193;              {mC2}
            cnt t 625, 248;
            cnt t 625, 282;
            cnt t 697, 248;

            cnt t 633, 313;              {m8}
            cnt t 673, 313;
            cnt t 633, 342;
            cnt t 673, 342;

            cnt t 653, 193;              {mB1}
            cnt t 653, 227;
            cnt t 688, 208;
lcm; iopad t 0, 0;
     iopad t 225, 0;
     iopad t 450, 0;
     iopad t 675, 0;
     iopad t 0, 225;
     iopad t 0, 450;
       box  110, 125  & 160, 140;  {Vin1 to m1}
       box  150, 140  & 160, 160;
       box  150, 160  & 180, 170;
       box  170, 170  & 180, 235;
       box  170, 235  & 203, 245;

       box  335, 125  & 350, 180;  {Vin2 to m2}
       box  350, 170  & 370, 180;
       box  360, 180  & 370, 200;
       box  210, 210  & 395, 220;  {m1-m2-m5}
       box  395, 210  & 405, 225;
       box  395, 225  & 450, 235;
       box  250, 200  & 260, 210;
       box  298, 200  & 308, 210;

       box  210, 260  & 266, 270;  {m1 to m4}
       box  290, 260  & 346, 270;
       box  230, 270  & 240, 330;
       box  320, 270  & 330, 330;
       box  210, 330  & 290, 340;
       box  300, 330  & 390, 340;
       box  380, 340  & 390, 460;
       box  360, 450  & 380, 460;
       box  320, 420  & 360, 460;

       box  125, 335  & 190, 350;  {VDD line}
       box  180, 350  & 190, 385;
       box  180, 385  & 350, 395;
       box  225, 395  & 235, 465;
       box  275, 395  & 285, 470;
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                box  275, 470  & 550, 480;
                box  550, 380  & 560, 480;
                box  560, 380  & 610, 390;
                box  600, 350  & 610, 380;
                box  590, 340  & 690, 350;
                box  590, 325  & 600, 340;
                box  550, 325  & 590, 335;
                box  560, 455  & 685, 465;

                box  125, 560  & 200, 575;  {Vout line}
                box  190, 500  & 200, 560;
                box  200, 500  & 705, 510;
                box  705, 310  & 715, 510;
                box  620, 310  & 705, 320;


                box  620, 290  & 630, 310;
                box  530, 280  & 635, 290;
                box  530, 290  & 540, 310;
                box  510, 310  & 540, 320;
                box  500, 300  & 510, 325;

                box  560, 125  & 575, 180;  {Vss line}
                box  575, 170  & 610, 180;
                box  600, 180  & 610, 205;
                box  525, 170  & 560, 180;
                box  515, 170  & 525, 200;
                box  430, 190  & 515, 200;
                box  460, 200  & 470, 280;
                box  460, 280  & 480, 290;
                box  470, 290  & 480, 325;
                box  430, 250  & 460, 260;
                box  545, 180  & 555, 210;

                box  675, 125  & 690, 180;  {Gnd line}
                box  660, 170  & 675, 180;
                box  650, 170  & 660, 190;
                box  640, 190  & 670, 200;
                box  480, 225  & 685, 235;  {mB2-mB1}
                box  490, 235  & 500, 260;
                box  685, 200  & 695, 235;

                box  530, 245  & 710, 255;  {mC1-mC2}

                box  430, 285  & 450, 295;  {m7 & m6}
                box  435, 295  & 445, 340;
                box  410, 305  & 435, 315;
                box  410, 315  & 420, 380;
                box  410, 380  & 455, 390;
                box  455, 380  & 465, 450;
                box  445, 430  & 455, 440;
        lcg;    box  330, 430  & 350, 450;
    end;
begin
```

```
    opamp;
    aa t 315,540;
    ss t 355,540;
    ff t 395,540;
    uofa t 445,540;
    year t 500,540;
end.
```

AHF PROGRAM FOR OP-AMP # 3

```
    {Layout description for cascode OA}
chip opampthree;

  symbol cnt;
    begin
        lcc;   box 0, 0 & 5, 5;
    end;

  symbol iopad;
    begin
        lcm;   box 0, 0 & 125, 125;
        lcg;   box 6, 6 & 119, 119;
    end;


symbol  opamp;
   begin

      lcpw; poly 400, 220 & 400, 350 &
                 620, 350 & 620, 370 &
                 735, 370 & 735, 310 &
                 780, 310 & 780, 220 ;

      lcf;  box  310, 250 & 360, 302;    {m1}
            box  310, 340 & 360, 392;    {m2}
            box  410, 380 & 510, 420;    {m3}
            box  550, 405 & 650, 445;    {m4}
            box  420, 240 & 520, 330;    {m5}
            box  420, 240 & 520, 330;    {m5}
            box  550, 240 & 650, 330;    {m6}
            box  280, 515 & 370, 560;    {m7}
            box  780, 360 & 820, 440;    {m8}
            box  675, 275 & 715, 322;    {m9}
            box  720, 244 & 765, 260;    {mc1}
            box  700, 400 & 716, 445;    {mc2}
            box  200, 515 & 230, 560;    {mb1}
            box  200, 460 & 219.5, 500; {mb2}
            box  280, 465 & 300, 485;    {sub}
            box  750, 510 & 770, 530;

      lcpg; poly 394, 214 & 394, 356 &
                 614, 356 & 614, 376 &
                 741, 376 & 741, 316 &
                 786, 316 & 786, 214;

      lcng; poly 390, 210 & 390, 360 &
                 610, 360 & 610, 380 &
```

```
                745, 380 & 745, 320 &
                790, 320 & 790, 210;

lccp;  box   455, 470 & 700, 535;    {cap}
       box   700, 500 & 710, 510;
       box   710, 495 & 730, 515;

lcp;   box   330, 190 & 350, 210;    {m1}
       box   330, 210 & 342, 310;
       box   190, 190 & 210, 210;    {m2}
       box   190, 210 & 200, 320;
       box   190, 320 & 330, 330;
       box   330, 320 & 342, 400;
       box   404, 395 & 520, 405;    {m3}
       box   520, 390 & 540, 410;
       box   530, 410 & 540, 420;    {m4}
       box   530, 420 & 656, 430;
       box   414, 265 & 656, 315;  {m5 - m6}
       box   194, 530 & 395, 545;  {m7 & mb1}
       box   795, 350 & 805, 520;    {m8}
       box   785, 520 & 805, 540;
       box   690, 265 & 700, 340;    {m9}
       box   655, 340 & 700, 350;
       box   635, 340 & 655, 360;
       box   737, 235 & 750, 270;    {mc1}
       box   737, 270 & 805, 280;
       box   805, 265 & 825, 285;
       box   670, 410 & 690, 430;    {mc2}
       box   690, 417 & 725, 430;
       box   195, 475 & 230, 485;    {mb2}
       box   230, 470 & 250, 490;
       box   425, 490 & 445, 510;    {cap}
       box   445, 495 & 460, 505;
       box   460, 475 & 694.5, 530;

lcnp;  box   290, 230 & 375, 415;
       box   425, 230 & 445, 250;
       box   495, 230 & 515, 250;
       box   555, 230 & 575, 250;
       box   625, 230 & 645, 250;

       poly  175, 445 & 175, 590 &
             410, 590 & 410, 500 &
             265, 500 & 265, 445;

       poly  390, 365 & 390, 460 &
             835, 460 & 835, 330 &
             760, 330 & 760, 385 &
             585, 385 & 585, 365;

lcpp;  box   295, 235 & 370, 410;
       box   425, 235 & 445, 250;
       box   495, 235 & 515, 250;
       box   555, 235 & 575, 250;
```

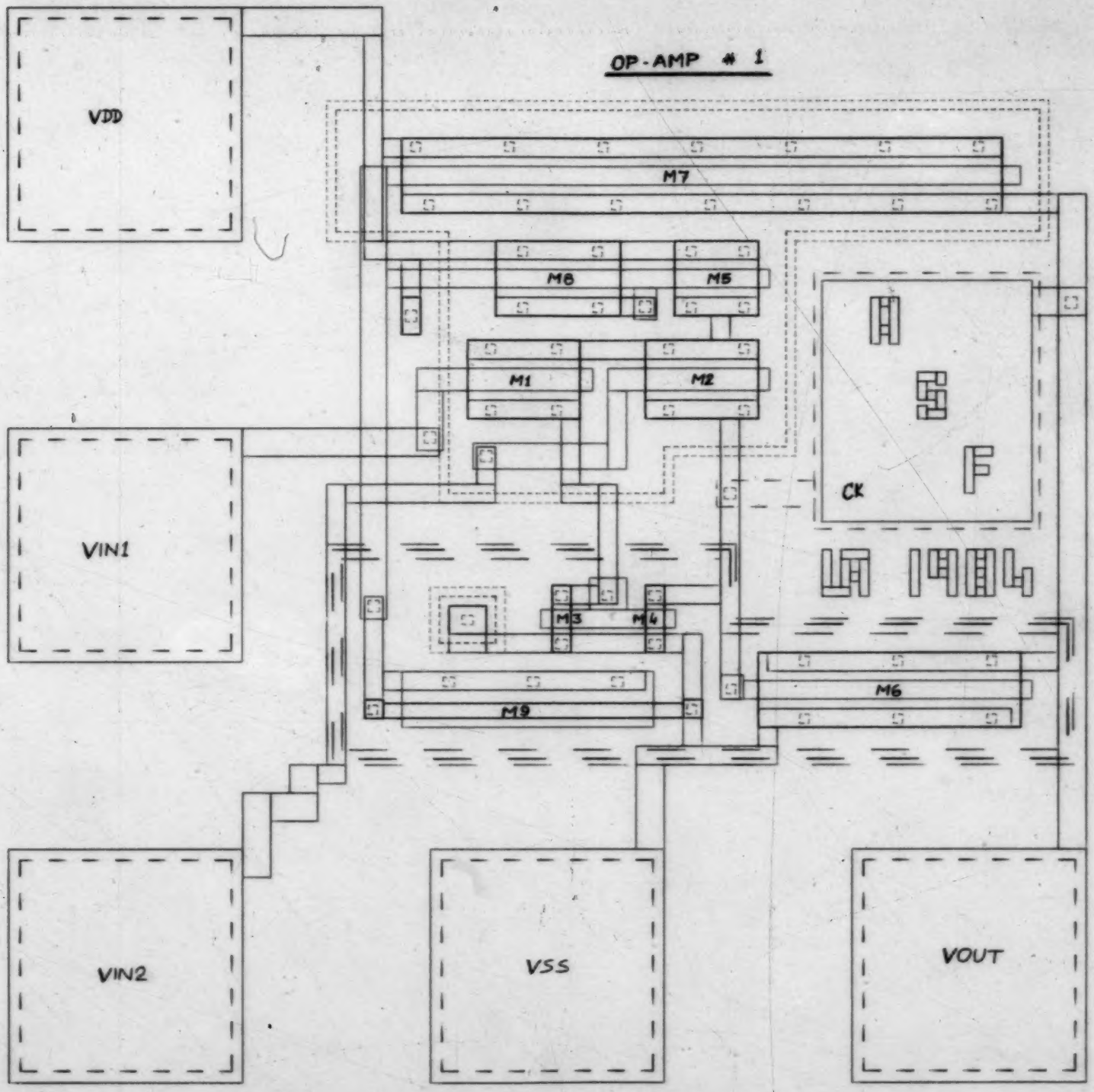
```
      box  625, 235 & 645, 250;
      poly 180, 450 & 180, 585 &
           405, 585 & 405, 505 &
           260, 505 & 260, 450;

      poly 395, 370 & 395, 455 &
           830, 455 & 830, 335 &
           765, 335 & 765, 390 &
           580, 390 & 580, 370;

lcc;  box    285, 473  & 295,  478; {Subst}
      box    757, 515  & 762,  525;
      box    432, 244  & 437,  256;
      box    503, 244  & 508,  256;
      box    562, 244  & 567,  256;
      box    633, 244  & 638,  256;


      cnt  t 197, 197;          {m1}
      cnt  t 340, 197;          {m2}
      cnt  t 313, 260;          {m1}
      cnt  t 313, 290;          {m1}
      cnt  t 352, 260;
      cnt  t 352, 290;

      cnt  t 313, 350;          {m2}
      cnt  t 313, 380;
      cnt  t 352, 350;
      cnt  t 352, 380;

      cnt  t 420, 383;          {m3}
      cnt  t 420, 412;
      cnt  t 450, 383;
      cnt  t 450, 412;
      cnt  t 490, 383;
      cnt  t 490, 412;

      cnt  t 527, 397;
      cnt  t 560, 408;          {m4}
      cnt  t 560, 438;          {m4}
      cnt  t 600, 408;
      cnt  t 600, 438;
      cnt  t 640, 408;
      cnt  t 640, 438;

      cnt  t 430, 322;          {m5}
      cnt  t 472, 322;
      cnt  t 510, 322;
      cnt  t 473, 253;
      cnt  t 532, 280;
      cnt  t 532, 302;

      cnt  t 600, 252;          {m6}
```

```
        cnt  t 560, 322;
        cnt  t 600, 322;
        cnt  t 640, 322;
        cnt  t 643, 347;

        cnt  t 290, 518;          {m7}
        cnt  t 290, 552;
        cnt  t 325, 518;
        cnt  t 325, 552;
        cnt  t 360, 518;
        cnt  t 360, 552;
        cnt  t 385, 535;

        cnt  t 792, 528;          {m8}
        cnt  t 783, 370;
        cnt  t 783, 400;
        cnt  t 783, 422;
        cnt  t 812, 370;
        cnt  t 812, 392;
        cnt  t 812, 422;
        cnt  t 812, 272;

        cnt  t 678, 282;          {m9}
        cnt  t 678, 312;
        cnt  t 707, 282;
        cnt  t 707, 312;
        cnt  t 705, 402;
        cnt  t 723, 250;

        cnt  t 757, 250;          {mc1}

        cnt  t 705, 437;          {mc2}
        cnt  t 717, 502;
        cnt  t 677, 420;

        cnt  t 212, 552;          {mb1-mb2}
        cnt  t 212, 518;
        cnt  t 208, 463;
        cnt  t 208, 492;
        cnt  t 238, 478;
        cnt  t 242, 535;

        cnt  t 433, 500;          {cap}

lcm;    iopad t 0,0;
        iopad t 225,0;
        iopad t 450,0;
        iopad t 675,0;
        iopad t 0, 225;
        iopad t 0, 450;

        box    335, 125  & 350,  210; {Vin1}
        box    110, 125  & 125,  140; {Vin2}
        box    125, 130  & 150,  140;
```

```
box     140, 140  & 150,  170;
box     150, 160  & 180,  170;
box     170, 170  & 180,  190;
box     180, 180  & 195,  190;
box     195, 180  & 205,  210;

box     125, 335  & 210,  350; {Gnd}
box     200, 350  & 210,  460;
box     200, 460  & 235,  470;
box     235, 460  & 245,  490;

box     125, 560  & 370,  575; {Vdd}
box     200, 550  & 230,  560;
box     260, 470  & 270,  560;
box     270, 470  & 300,  480;
box     280, 550  & 370,  560;
box     370, 565  & 810,  575;
box     810, 265  & 820,  575;
box     765, 500  & 810,  510;
box     755, 500  & 765,  530;

box     560, 125  & 575,  220; {Vss}
box     530, 210  & 560,  220;
box     530, 220  & 540,  250;
box     420, 250  & 685,  260;
box     430, 240  & 440,  250;
box     500, 240  & 510,  250;
box     560, 240  & 570,  250;
box     630, 240  & 640,  250;
box     675, 260  & 685,  430;

box     785, 125  & 800,  210; {Vout}
box     730, 210  & 800,  220;
box     780, 220 & 790, 440;
box     720, 210  & 730,  275;
box     715, 275  & 730,  290;
box     705, 275  & 715,  400;
box     700, 400  & 715,  410;

box     310, 250  & 320,  515;{m1-m2}
box     280, 515  & 370,  525;
box     350, 250  & 360,  302;
box     360, 270  & 380,  280;
box     380, 270  & 390,  410;
box     380, 410  & 510,  420;

box     410, 380  & 510,  390;{m3-m5}
box     420, 320  & 530,  330;
box     530, 270  & 540,  395;
box     520, 395  & 540,  405;
box     450, 330  & 460,  380;

box     350, 340  & 360,  435;{m4-m6}
box     350, 435  & 650,  445;
```

```
                box     350, 445  & 360,  455;
                box     335, 455  & 375,  495;
                box     550, 405  & 650,  415;
                box     580, 330  & 590,  405;
                box     550, 320  & 650,  330;
                box     640, 330  & 650,  360;

                box     700, 435  & 745,  445;{m4-m6}
                box     715, 445  & 725,  515;
                box     735, 320  & 745,  435;
                box     735, 310  & 755,  320;
                box     755, 244  & 765,  320;
                box     380, 530  & 395,  545;
                box     380, 545  & 790,  555;
                box     790, 520  & 800,  555;
                box     200, 490  & 220,  500;{mb1-mb2}
                box     205, 500  & 215,  515;
                box     200, 515  & 250,  525;
                box     240, 525  & 250,  545;
                box     430, 445  & 440,  510;{cap}

    lcg;        box     345, 465  & 365,  485;
  end;
begin
  opamp;
end.
```

OP-AMP # 1

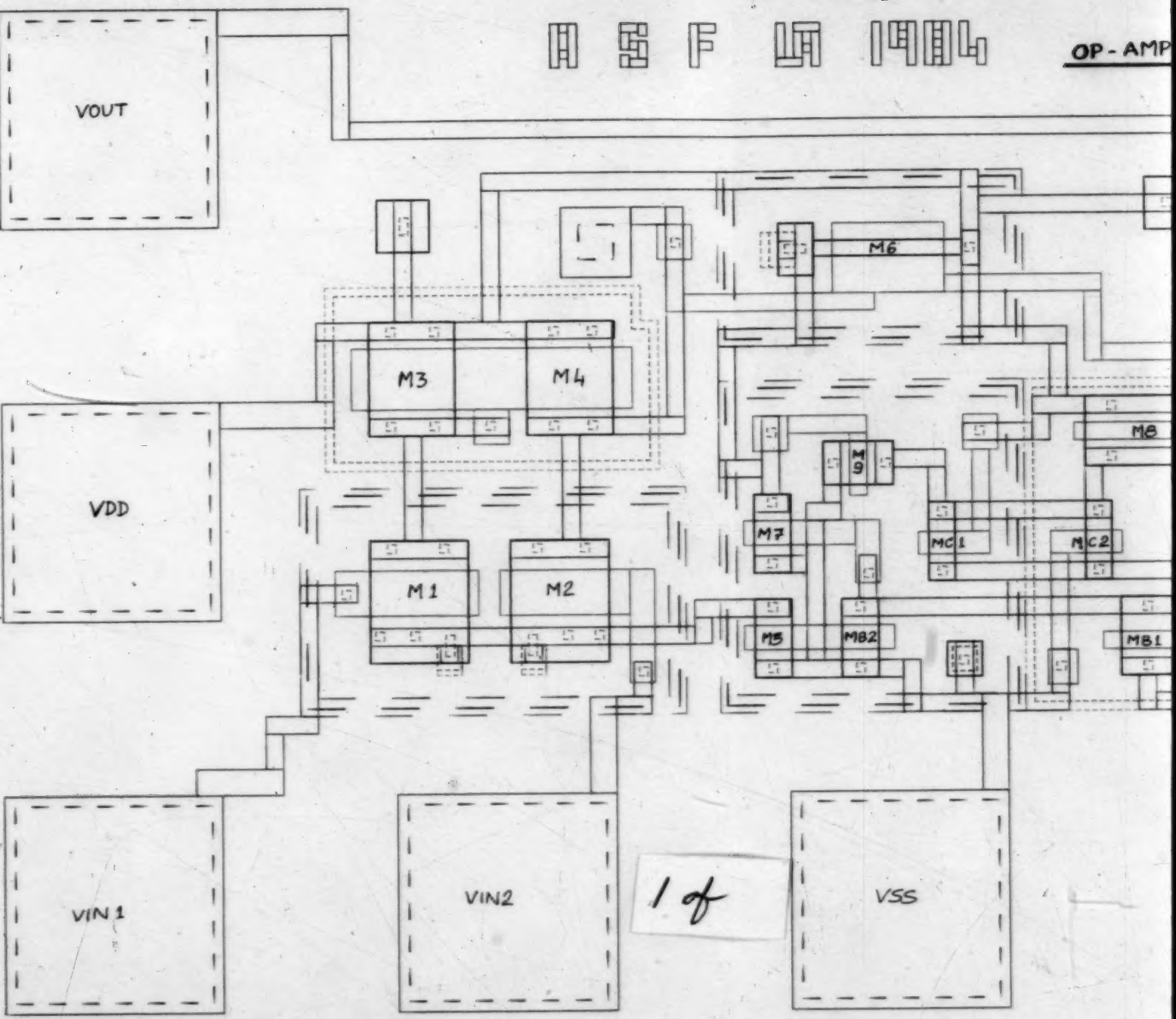


COLOURS EXPLAINED

IN PAGE 128

MOS IN 1984

OP-AMP



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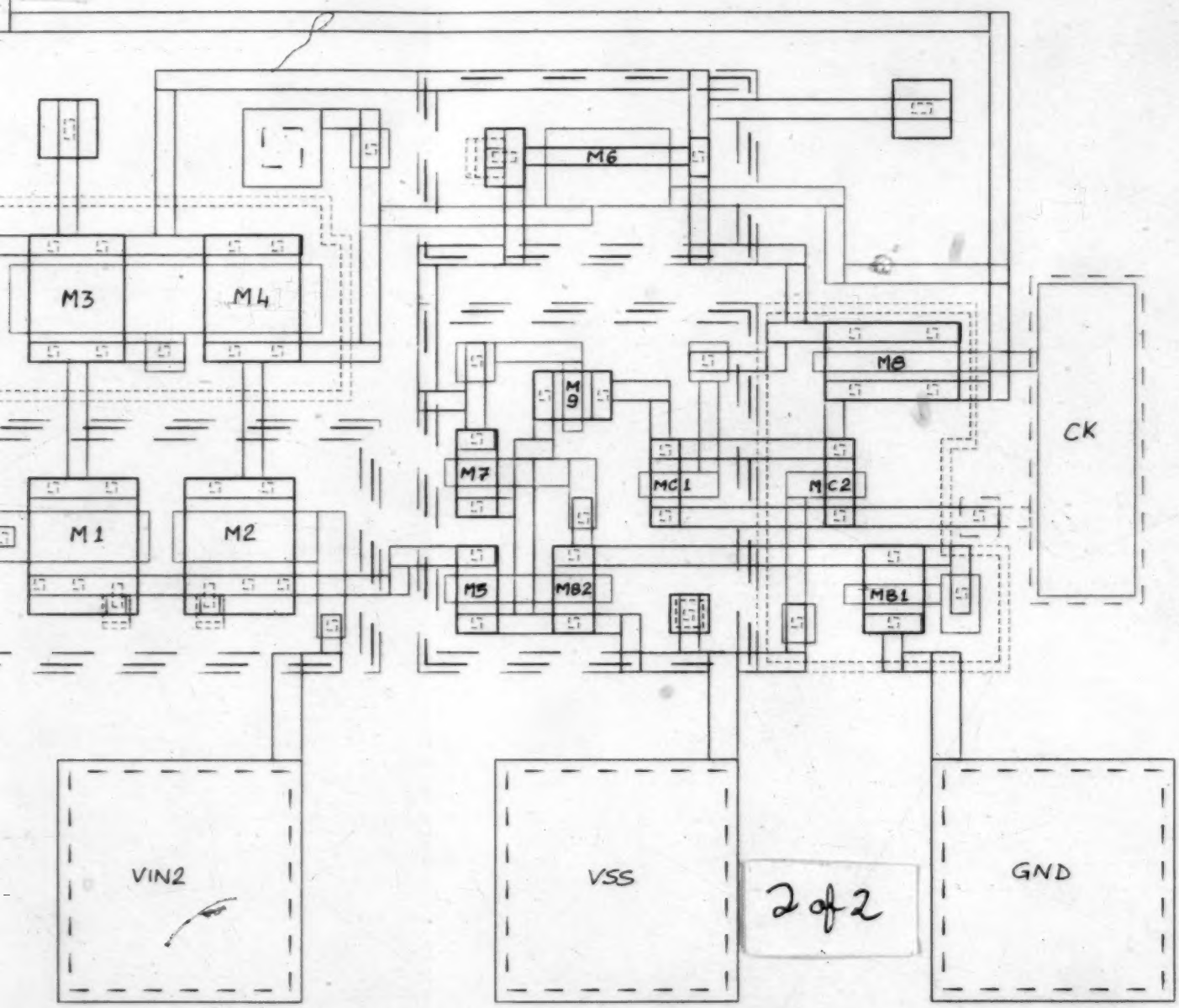
COLOURS EXPLAINED
IN PAGE 128

MSFM 1984

OP-AMP # 2



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EXPLAINED

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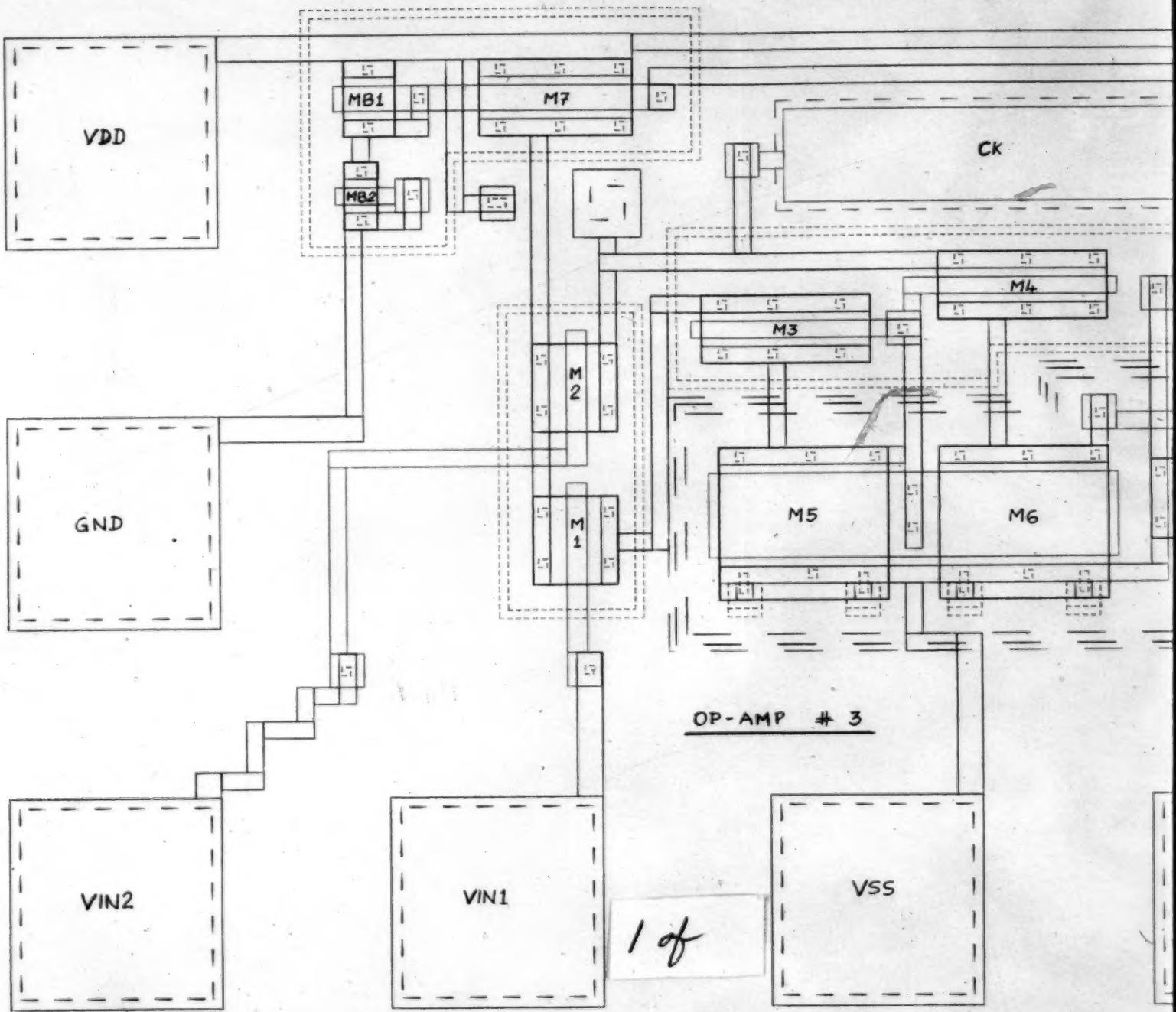
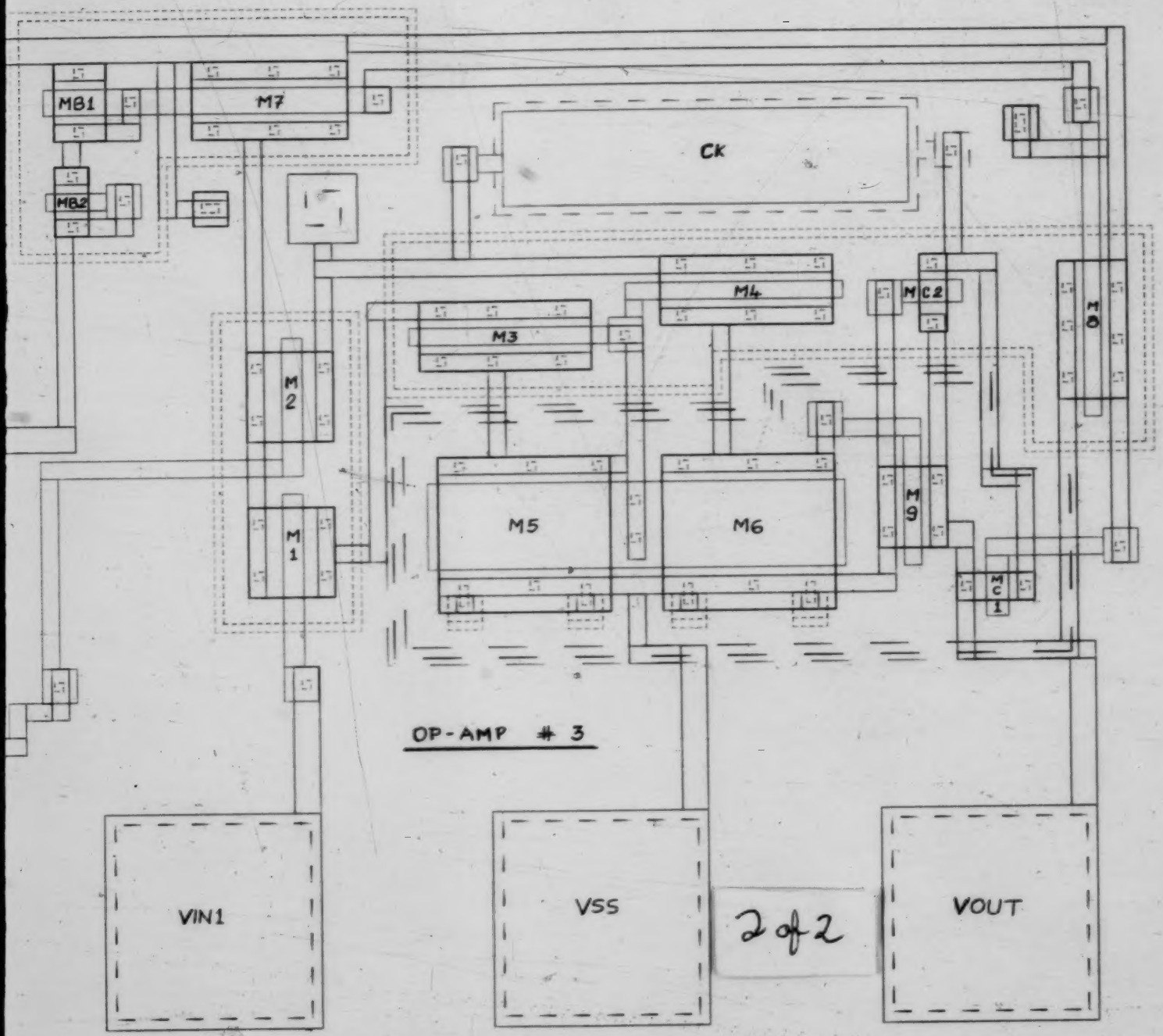


OP-AMP # 3

1 of

COLOURS EXPLAINED
IN PAGE 128



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COLOURS EXPLAINED IN PAGE 128